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Design of an Ultra-Wideband LDMOS High-Efficiency Power Amplifier with Integrated Filtering Matching

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ABSTRACT: The rapid evolution of wireless communication networks is driving the rapid development of communication systems toward greater integration, wider bandwidth, and higher efficiency. To satisfy the design requirements of broadband, high-efficiency power amplifiers, this study proposes an implementation scheme that integrates filtering, matching, and harmonic-control technologies. In this innovative method, high-order matching networks are converted into low-order passive networks that integrate the parasitic output capacitance and package inductance of transistors, thereby achieving a more compact area. In addition, a dual-stub microstrip line cascaded topology is introduced to suppress the second harmonic. The test results demonstrate that the power amplifier achieves a gain of more than 16.5 dB in the 100–900 MHz frequency band, maintains a drain efficiency of over 55%, with a peak drain efficiency of up to 75% under saturated operation, delivers a saturated output power of 40.5–42 dBm, achieves a second harmonic suppression of up to 61 dBc, and has a relative bandwidth of 160%. This design realizes high-efficiency power transmission performance and demonstrates excellent potential for engineering applications in communication systems.

1. INTRODUCTION

With the development of wireless communications, broadband high-efficiency radio-frequency (RF) power amplifiers have long been a research focus in communication. They are required to cover the bandwidth of high-speed signals and support multiple frequency bands. Currently, 5G technology has enabled higher-rate signals and more abundant frequency bands [1, 2], which means that the design of RF systems must expand bandwidth. Moreover, among the most energy-consuming components, power amplifiers account for 44% of the total energy consumption. Therefore, system energy consumption has become a key issue affecting carbon emissions in the communication industry [3]. Under these circumstances, improving the efficiency of RF systems is crucial. As one of the components with the highest power consumption in RF systems [4], broadband high-efficiency power amplifiers have become a key design objective for researchers and engineers to achieve.

To address the energy consumption issues of 5G communications, enhancing the efficiency and bandwidth of power amplifiers is critical; therefore, various switching-mode power amplifiers have drawn considerable attention. By reducing the overlapping interval between the alternating voltage and current waveforms at the output of RF transistors, switching-mode power amplifiers, such as Class E and Class F, can significantly reduce power consumption and achieve high-efficiency signal amplification. Although Class E and F power amplifiers are capable of delivering high efficiency, they face challenges in broadband design [5, 6]. Continuous Class F and continuous inverse Class F modes can meet not only high-efficiency requirements but also broadband amplification [7]. However, their harmonic impedance control networks require precise regulation of the second- and third-order harmonics. Controlling third-order harmonics yields limited improvements in amplifier performance while increasing circuit design complexity. Wright et al. proposed a design methodology for Class J power amplifiers, which involves setting the second-harmonic impedance on the imaginary axis of the Smith chart to achieve broadband characteristics [8]. Guo et al. realized third-harmonic control using a band-pass filter, achieving a power-added efficiency (PAE) of 70.9% at a frequency of 2.4 GHz [9]. Chen and Peroulis implemented fourth-harmonic control via a low-pass filtering matching network, attaining a PAE of 82% at 3.1 GHz [10]. In [11], a power of 47.3 dBm and an efficiency ranging from 65% to 75% were achieved over the frequency band of 1.0–1.5 GHz by utilizing a low-pass filtering matching network. To realize system miniaturization, research efforts have been devoted to the co-design of multiple RF components, such as developing filtering baluns and filtering power amplifiers [12–16]. This integrated design approach reduces the circuit footprint and mitigates transmission loss and signal reflection caused by mismatches between RF components. However, notable limitations remain: the dedicated matching networks of filtering power amplifiers suffer from insufficient design flexibility, restricting bandwidth expansion; harmonic-tuned power amplifiers mostly require precise regulation of multi-order harmonics, which easily increases circuit complexity and fails to effectively integrate with filtering functionality; traditional broadband matching methods require multiple circuits to achieve different frequency bands, which increases the number of components and reduces the reliability of the system;

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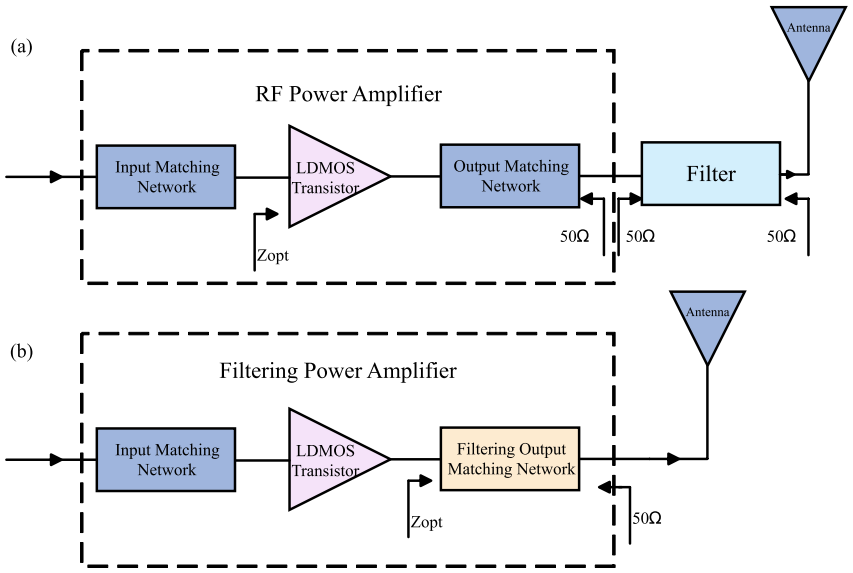

FIGURE 1. (a) Cascaded structure of power amplifier and filter. (b) Structure of filtering power amplifier.

and the filtering power amplifier with a single band of harmonics is difficult to achieve methods struggle to balance the design requirements of the impedance transformation ratio and bandwidth and fail to incorporate transistor parasitic parameters into the network synthesis framework, which is prone to causing issues such as impedance mismatch and power loss.

To address the aforementioned issues, this paper proposes a synthesis method for filtering matching networks tailored for broadband high-efficiency power amplifiers. Unlike conventional filtering power amplifiers, the proposed synthesis method incorporates the transistor's output parasitic capacitance and package parasitic inductance directly into the matching network synthesis process via T-network equivalent transformation, achieving broadband impedance matching and filtering functionality within a unified synthesis framework. Furthermore, the synthesized network requires only second-harmonic control to avoid complex multi-harmonic tuning while maintaining high efficiency. Finally, a 100–900 MHz broadband prototype was designed and fabricated, which validates the feasibility of the proposed design methodology and demonstrates that the proposed network synthesis method enables broadband impedance matching and high-efficiency operation.

2. DESIGN OF THE FILTERING POWER AMPLIFIER

In the radio-frequency (RF) front-end module, both the filter and RF power amplifier play pivotal roles. Specifically, the RF power amplifier is responsible for amplifying the power of RF signals, and the filter can effectively suppress spurious signals (e.g., harmonic components) to achieve frequency-band filtering and channel selection. The two components can be cascaded in a conventional design as illustrated in Fig. 1(a), wherein the power amplifier and filter are configured separately, with all ports matched to 50 Ω before cascading. Although the conventional design structure can suppress the nonlinear effects of the power amplifier, optimize the signal spectrum, and reduce interference, it still has two prominent drawbacks: first, impedance mismatch tends to occur between devices, which consequently leads to signal reflection and power loss; second, the layout with discrete packages occupies a large space, which fails to meet the miniaturization requirements of the RF equipment. To address these issues, in this study, a filter is directly employed as the output matching network of the power amplifier. This realizes an integrated collaborative design of the filter and power amplifier, and the corresponding circuit structure is depicted in Fig. 1(b).

2.1. T-Π Network Equivalent Transformation Theory

As shown in Fig. 2, the two-port T-network consists of an inductor L_1 and a capacitor C_3 connected in parallel, which are then connected in series with an inductor L_2. In accordance with the calculation criteria for two-port networks, this network can be represented by an $ABCD$ transmission matrix.

The transmission matrix of the T-network is finally derived as follows:

$$\begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} = \begin{bmatrix} 1-\omega^2 L_1 C_3 & j\omega\,(L_1+L_2)-j\omega^3 L_1 L_2 C_3 \\ j\omega C_3 & 1-\omega^2 L_2 C_3 \end{bmatrix} \tag{1}$$

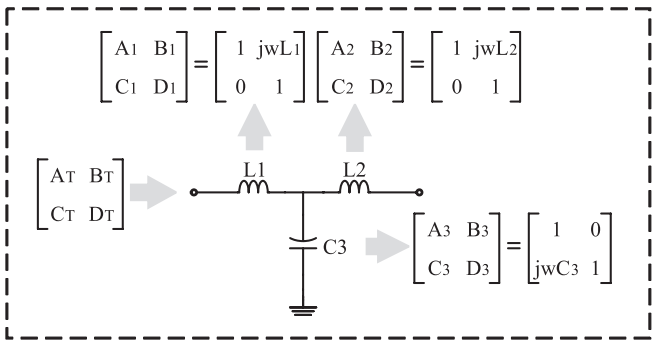

FIGURE 2. Two-port T-network.

transmission matrix.

By the same reasoning, the two-port Π-network depicted in Fig. 3 can be expressed using the $ABCD$ transmission matrix as follows:

$$\begin{bmatrix} A_\Pi & B_\Pi \\ C_\Pi & D_\Pi \end{bmatrix} = \begin{bmatrix} 1-\omega^2 L_x C_z & j\omega L_x \\ j\omega\,(C_y+C_z)-j\omega^3 C_y C_z L_x & 1-\omega^2 L_x C_y \end{bmatrix} \tag{2}$$

To realize the equivalent replacement of the two-port T-network with the Π-network, the transmission matrices of the two networks can be equated: by setting L_1=L_2,

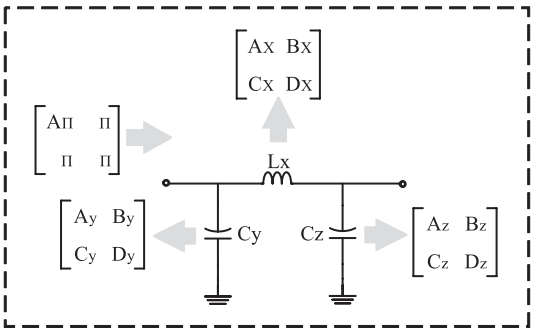

FIGURE 3. Two-port Π-network.

$$L_x = 2L_1 - \omega^2 L_1^2 C_3 \tag{3}$$

$$C_y = C_z = \frac{L_2 C_3}{L_x} \tag{4}$$

The above transformation is derived based on the $ABCD$-parameter equivalence between the T-type and Π-type networks. Therefore, the transformed network preserves the same input-output transmission characteristics as the original network at the design frequency. Since the $ABCD$ parameters are frequency-dependent, the equivalent relationship is mainly maintained within the target operating bandwidth of 100–900 MHz, where the transmission characteristics vary smoothly.

2.2. Π-Microstrip Line Section Equivalent Transformation Theory

As shown in Fig. 4, for a transmission line with a characteristic impedance of Z_0, propagation constant of β, and length L, the $ABCD$ transmission matrix can be calculated by establishing the voltage-current relationship.

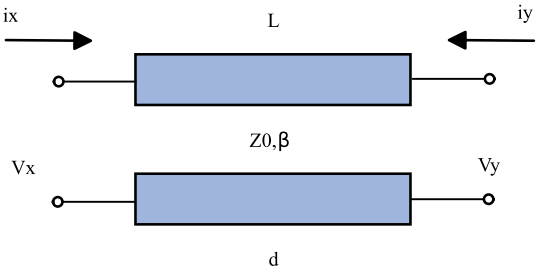

FIGURE 4. Schematic diagram of the microstrip line section.

For an open-circuited stub, the voltage and current can be expressed as follows:

$$V(d) = 2V^+ \cos(\beta d), \quad I(d) = \frac{2jV^+}{Z_0}\sin(\beta d) \tag{5}$$

For a short-circuited transmission line section, the voltage and current can be expressed as follows:

$$V(d) = 2jV^+ \sin(\beta d), \quad I(d) = \frac{2V^+}{Z_0}\cos(\beta d) \tag{6}$$

After calculation, the $ABCD$ transmission matrix of the microstrip line can be expressed as follows:

$$\begin{bmatrix} A_L & B_L \\ C_L & D_L \end{bmatrix} = \begin{bmatrix} \cos(\beta L) & jZ_0 \sin(\beta L) \\ \frac{j\sin(\beta L)}{Z_0} & \cos(\beta L) \end{bmatrix} \tag{7}$$

To realize the equivalent replacement of the Π-network with the microstrip line section, the two transmission matrices can be equated. Finally, by setting C_y=C_z, we obtain:

$$Z_0 = \frac{\omega L_x}{\sin(\beta L)} \tag{8}$$

$$\beta L = \arccos(1-\omega^2 L_x C_y) \tag{9}$$

It should be noted that the Π-network to microstrip-line transformation is also a frequency-dependent equivalent process. The characteristic impedance and electrical length are determined at the selected reference frequency, and the equivalence accuracy may gradually degrade when the operating frequency deviates from this reference frequency. In this work, 500 MHz is selected as the reference frequency because it is close to the center frequency of the target 100–900 MHz bandwidth.

2.3. Synthesis Method of the Filtering Matching Network

Most existing broadband matching methods fail to balance high impedance transformation ratios and wide bandwidths, and traditional high-order broadband matching network occupies significant circuit area. To address this trade-off between bandwidth and network order, this study proposes an integrated filtering network synthesis scheme. The proposed design method is based on a high-order Butterworth low-pass filter prototype [17]. Owing to its maximally flat passband response [18] and smooth impedance variation, the Butterworth prototype provides a stable starting point for the subsequent T–Π network transformation and transistor parasitic absorption adopted in this work. Therefore, it is selected as the initial prototype of the proposed filtering matching network. This work integrates transistor parasitic parameters into the matching network, achieving broadband real-to-complex impedance matching. Figs. 5(a)–5(g) demonstrate the step-by-step synthesis process of the proposed design, with detailed methods provided below.

Step 1: Using the impedance transformation ratio, relative bandwidth, center frequency, and maximum allowable in-band ripple as the core design indicators, we strictly followed

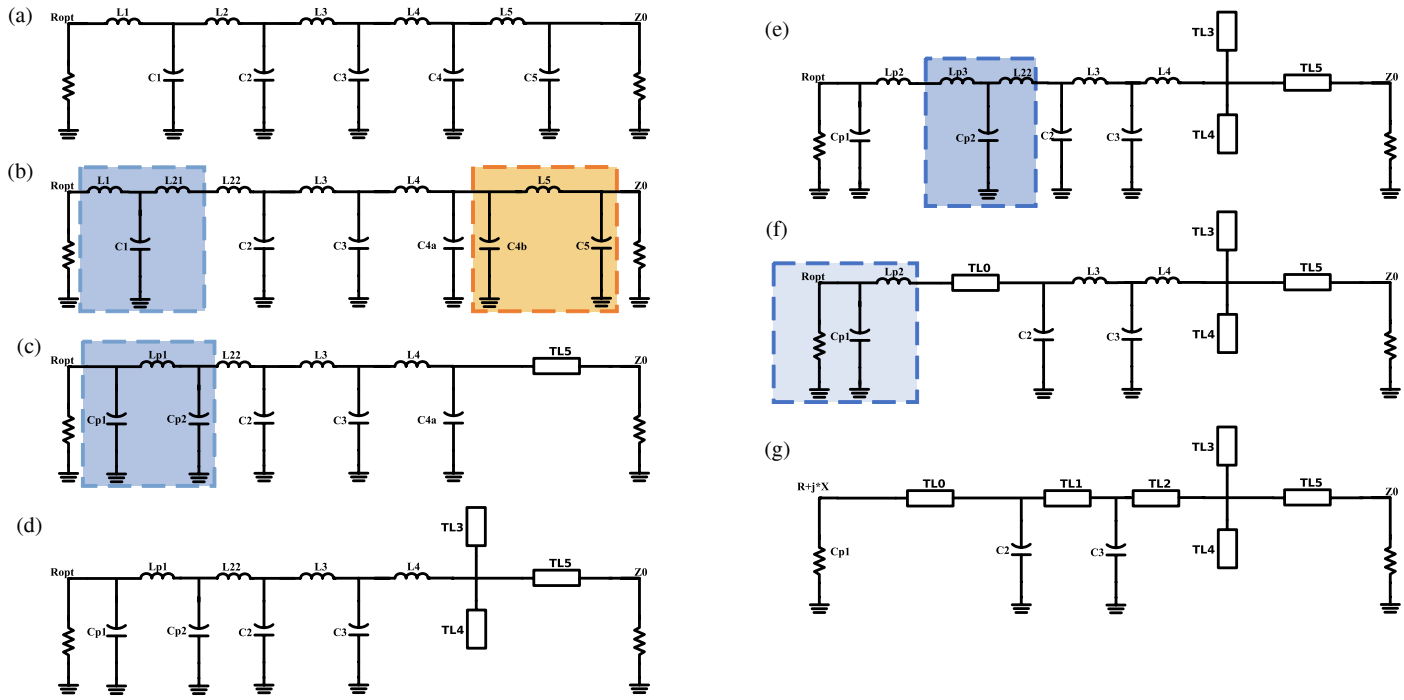

FIGURE 5. Synthesis process of the filtering matching network design. (a) Original network, (b) network decomposition into T-type and ∏-type configurations, (c) equivalent network transformation, ∏-type microstrip line transformation, (d) shunt capacitance-to-open-circuited microstrip line conversion, (e) re-decomposition into T-type configuration, (f) equivalent network transformation and matching point equivalence, and (g) lumped inductance-to-distributed parameter conversion.

the established method presented in [19] to sequentially complete processes of querying and denormalizing the normalized component values and construct a real-domain low-pass matching network. For demonstration purposes, the fifth-order maximum-order matching network provided in [19] was selected as an example, and the corresponding initial network topology is shown in Fig. 5(a).

Step 2: Perform parameter reconstruction on the network components L_1, L_2, and C_1 obtained in Step 1, so that they can equivalently simulate the inherent parasitic output capacitances and parasitic inductances of actual transistors. To enable the Π-network in Fig. 5(c) to replace the T-network in Fig. 5(b),

It is required that their A-parameters be equal, namely:

$$\begin{cases} 1-\omega^2 L_1 C_1 = 1-\omega^2 L_{p1} C_{p2} \\ j\omega\left(L_1+L_{21}\right) - j\omega^3 L_1 L_{21} C_1 = j\omega L_{p1} \\ j\omega C_1 = j\omega\left(C_{p1}+C_{p2}\right) - j\omega^3 C_{p1} C_{p2} L_{p1} \\ 1-\omega^2 L_{21} C_1 = 1-\omega^2 L_{p1} C_{p1} \end{cases} \tag{10}$$

In the T-Π equivalent transformation circuit, the initial values of inductor L_1, inductor L_{2a}, and capacitor C_1 were determined in the first-step calculation. Based on this, inductors L_{P1}, capacitors C_{P1}, and capacitor C_{P2} can be obtained by solving Eq. (10), thereby completing the T-Π equivalent transformation from Figs. 5 (b) to (c). Note that when splitting the inductor L_2 into two components (L_{2a} and L_{2b}), a reasonable value should be assigned to L_{2a} to ensure that the capacitor C_{P1} parameter required by the actual transistor can be achieved.

For the Π-type network enclosed by the box in Fig. 5(b), the equivalent replacement of the Π-type lumped parameters with the series microstrip line TL_5 can be realized using Eqs. (8) and (9).

Step 3: Based on the principle of the Richards transformation, the shunt capacitor C_{4a} can be equivalently replaced by two parallel open-circuited transmission lines, namely TL_3 and TL_4, as shown in Fig. 5(d). Because the Richards transformation is frequency-dependent, the center frequency of 500 MHz within the target bandwidth was selected as the design reference for converting the lumped-element model to the distributed counterpart, which provided an initial distributed implementation scheme for subsequent network synthesis. It should be noted that the Richards transformation is employed only to obtain the distributed implementation of the synthesized lumped-element network.

Step 4: Decompose inductor L_{P1} into the inherent package parasitic inductor L_{P2} of the transistor and residual inductor L_{P3}. Based on the equivalent conversion method of A-parameters between the T-network and microstrip line, the box-selected T-type topology in Fig. 5(e) can be converted into a microstrip line configuration, thereby effectively reducing the difficulty of soldering the actual transistor.

Step 5: In the impedance matching design, the optimal impedance, parasitic output capacitance, and package parasitic inductance are treated as an integrated parameter set; for the package-level output impedance derived from the load-pull

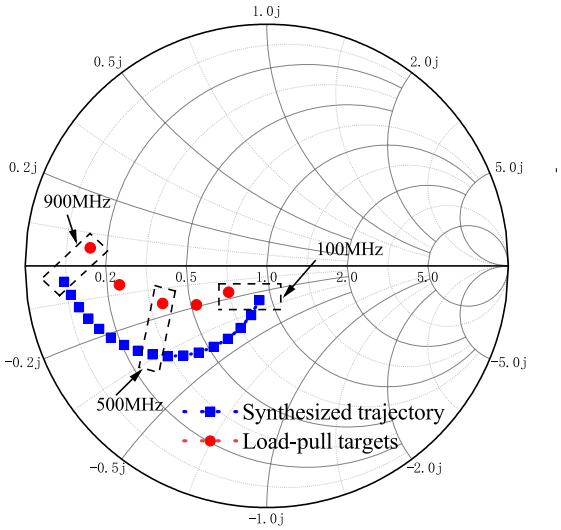

FIGURE 6. Comparison between intrinsic load-pull targets and synthesized fundamental impedance trajectory.

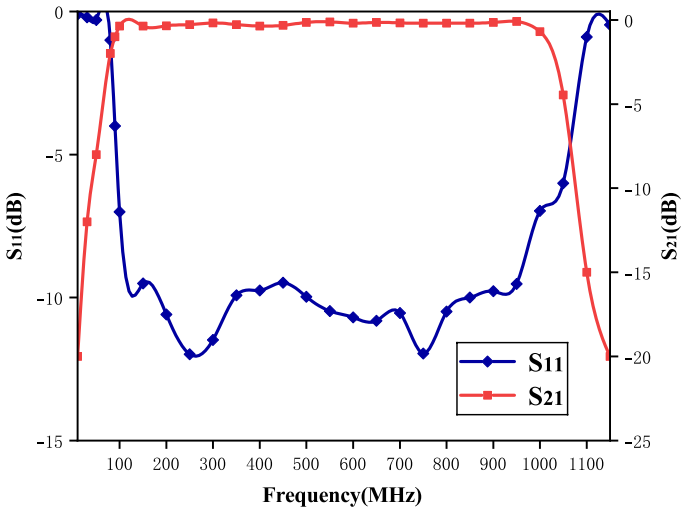

FIGURE 7. S-parameters (S_{11}, S_{21}) of the output matching network with filtering structure.

technique, the parameters C_{P1} and L_{P2} can be adjusted accordingly to ensure that

$$R = \frac{R_{\text{opt}}}{1+\omega^2 {C_{P1}}^2 {R_{\text{opt}}}^2} \tag{11}$$

$$X = \omega(L_{P2} - C_{P1} R_{\text{opt}}^2) \tag{12}$$

Finally, this study converts lumped inductors L_3 and L_4 into a series microstrip structure to reduce fabrication errors, while keeping capacitors as lumped components. This design improves circuit flexibility and facilitates debugging and optimization against transistor model deviations and manufacturing tolerances.

Based on the aforementioned transformation procedures, the original fifth-order low-pass matching network is reconstructed into a compact filtering matching network consisting of microstrip sections and capacitors. During this process, the equivalent transformation preserves the impedance characteristics of the original network while reducing the network order and physical complexity. The impedance trajectories of the original and transformed networks exhibit consistent variations within the 100–900 MHz bandwidth, verifying the effectiveness of the proposed synthesis method. In addition, the synthesized matching network achieves a non-monotonic broadband reactance trajectory, which is beneficial for maintaining the required impedance transformation over a wide frequency range. This characteristic originates from the combined effects of transistor parasitic parameters, equivalent network transformations, and the distributed implementation of the matching network, rather than a conventional passive filter response. To further clarify the relationship between the intrinsic impedance requirements of the transistor and the matching network, Fig. 6 compares the load-pull target impedances with the synthesized fundamental impedance trajectory. The results demonstrate that the proposed matching network achieves the desired impedance evolution over the 100–900 MHz bandwidth, thereby realizing the required non-monotonic reactance characteristic. Fig. 7 shows the S-parameters of the output matching network with a filtering structure. Unlike conventional networks, this integrated network employs frequency-selective impedance transformation, which simultaneously achieves fundamental matching and suppresses the second-harmonic component, thereby embedding filtering functionality into the matching topology. The proposed network exhibits a band-pass filtering response from 100 to 900 MHz. Within the passband, the insertion loss is close to 0 dB, and the return loss is better than 10 dB. Out-of-band rejection is better than about 10 dB above 900 MHz and about 7 dB below 100 MHz. Therefore, the proposed network can be regarded as a band-pass filtering matching network that simultaneously provides impedance matching and filtering characteristics.

3. DESIGN OF HARMONIC SUPPRESSION NETWORK

The core working mechanism of a harmonic-controlled power amplifier relies on the precise regulation of harmonic components. By altering the phase relationship between the device's internal voltage and current waveforms to achieve an interleaved distribution, this design can effectively reduce the loss of DC input power, thereby significantly improving the amplifier's overall efficiency. Among the various technical schemes for harmonic-controlled power amplifiers, class-J and continuous class-F power amplifiers have been widely adopted in engineering practices because of their excellent performance. Notably, the technical advantages of class-J power amplifiers stem from the expanded optimization of the impedance space for the fundamental and second-order harmonics. This design simultaneously achieves the dual goals of bandwidth extension and efficiency enhancement, with specific expressions for the fundamental and second-order harmonic impedances, as given in Eq. (13).

$$\begin{cases} Z_J(f_1) = R(1+j) \\ Z_J(f_2) = -jR(3\pi/8) \end{cases} \tag{13}$$

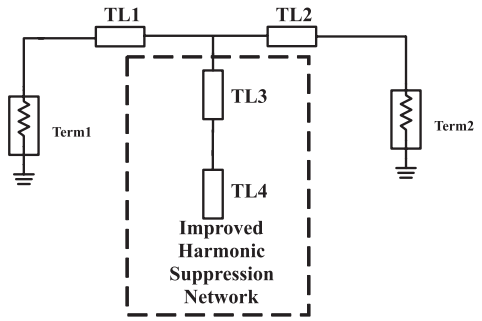

FIGURE 8. The structure of the improved harmonic suppression network.

where R represents the load impedance of the class-J power amplifier (PA). In contrast to conventional class-F power amplifiers, the continuous class-F topology extends the bandwidth range by optimizing the impedance-matching network, thus successfully breaking through the bottleneck in which bandwidth enhancement and efficiency optimization are mutually restricted in traditional class-F power amplifiers. The calculation formulas for the harmonic impedances of the continuous class-F power amplifier are expressed in Eq. (14).

$$\begin{cases} Z_F(f_1) = R_{Opt}\frac{2}{3} + \mathrm{j}R_{Opt}\gamma \\ Z_F(f_2) = -\mathrm{j}R_{Opt}\frac{7\sqrt{3}\pi}{24}\gamma \\ Z_F(f_3) = \infty \\ R_{Opt} = \frac{2V_{dc}}{I_{\max}} \end{cases} \tag{14}$$

where R_{Opt} denotes the optimal load impedance of the power amplifier; γ, serving as the bandwidth extension factor, is generally set within the range of $[-1, 1]$; V_{dc} represents the quiescent bias voltage of the power amplifier; $I_{\max}$ is the maximum bias current during device operation. Based on the voltage and current waveforms, the device was terminated with harmonics only up to the third order. This is because extending harmonic tuning beyond the third order would increase the circuit complexity and insertion loss of the load network [20] without a significant improvement in efficiency. Moreover, considering that the third- and higher-order harmonics contribute minimally to th efficiency of power amplifier. Based on this, the harmonic-controlled power amplifier proposed in this study was designed to regulate only the second-order harmonics. Combining the theoretical derivations of Eqs. (13) and (14), it can be concluded that compressing the overlapping range of voltage and current waveforms can effectively reduce the ineffective consumption of DC power, thereby achieving the optimization and enhancement of power amplifier efficiency.

To suppress harmonics and improve amplifier efficiency, a harmonic control network was integrated at the amplifier's drain output in this design. By adopting a cascaded structure of dual-stub microstrip lines, this topology differs from the traditional T-type matching network and significantly enhances its flexible adaptability. By optimizing the signal transmission path, this structure can achieve maximum fundamental-wave transmission and efficient second-harmonic reflection, thus enabling the power amplifier to operate with high performance and stability. Fig. 8 illustrates the structure of the improved harmonic suppression network. Fig. 9 shows the synthesized fundamental, second-harmonic impedance trajectories normalized to 50 Ω over the 100–1800 MHz band.

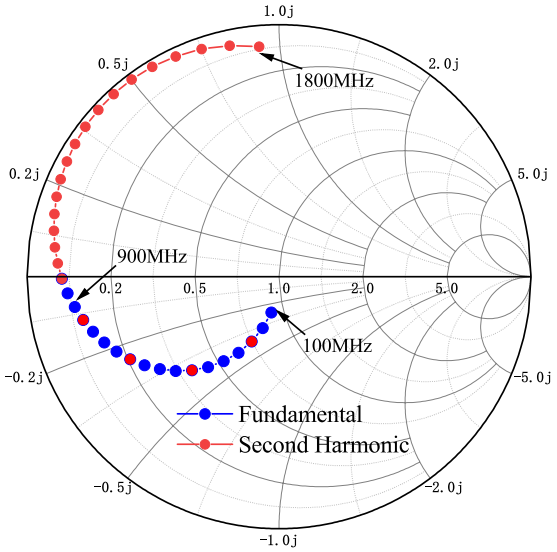

FIGURE 9. Simulated synthesized fundamental and second-harmonic impedance trajectories of the improved structure.

4. LAYOUT DESIGN AND MEASUREMENT

4.1. PA Simulation and Hardware Design

Based on the above theoretical analysis, this paper designs a 100–900 MHz broadband high-efficiency power amplifier using Advanced Design System (ADS). The proposed power amplifier employs an LDMOS transistor independently developed by the Chinese Academy of Sciences. The transistor features $Vds = 28\,\mathrm{V}$, $Vgs = 1.9\,\mathrm{V}$, and $Idq = 100\,\mathrm{mA}$, corresponding to Class AB operation. Under this bias condition, harmonic impedance control is implemented via the designed integrated matching network, which further enhances the drain efficiency of the power amplifier. The overall circuit is shown in Fig. 10. This design incorporates two auxiliary modules: First, the negative feedback network employs an RLC hybrid topology to improve the gain flatness within the 100–900 MHz band and ensure the stability of the power amplifier over the entire frequency range. To verify its effectiveness, Fig. 11 presents the simulated results of the stability factor K and the μ-factor obtained with the feedback network. As shown, both K and μ are greater than 1 across the full band, thereby satisfying the unconditional stability criteria. Second, the additional lumped/distributed network after the output matching network (OMN) serves as an auxiliary matching module, which is used to debug and optimize the output port impedance-matching characteristics of the power amplifier, compensate for the impedance deviation caused by device parasitic parameters and substrate effects, further improve the fundamental power transmission efficiency, and finally achieve better saturated output power.

For experimental verification, an FR-4 dielectric substrate was selected, with a dielectric constant of 4.5, loss tangent of 0.037, and thickness of 1 mm. This substrate selection fea-

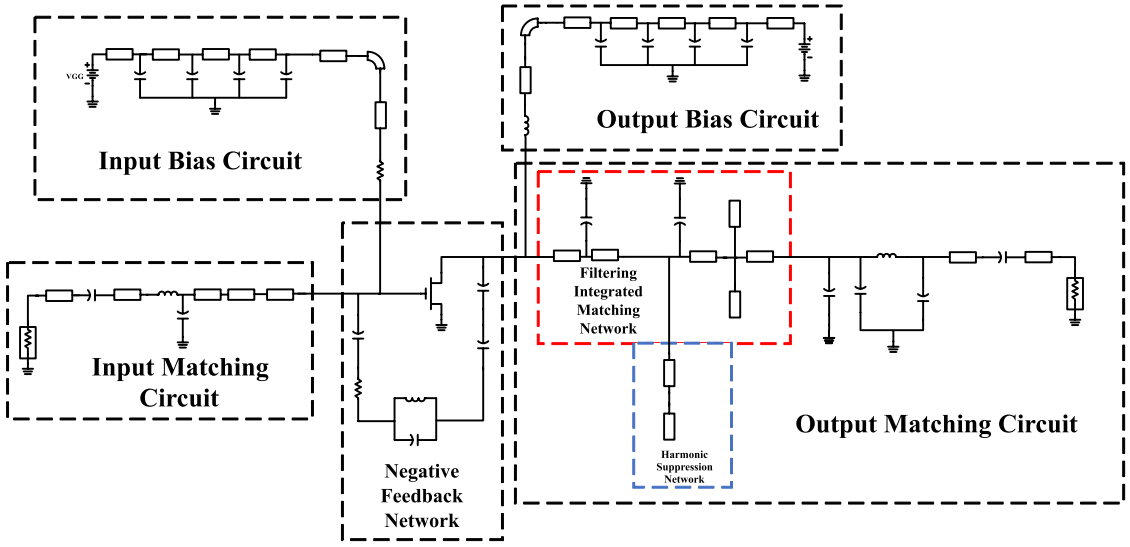

FIGURE 10. Overall circuit schematic diagram.

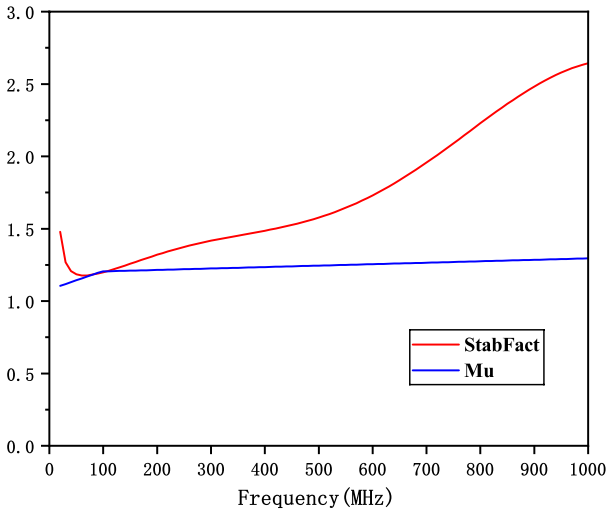

FIGURE 11. Simulated stability factor K and μ-factor with the negative feedback network.

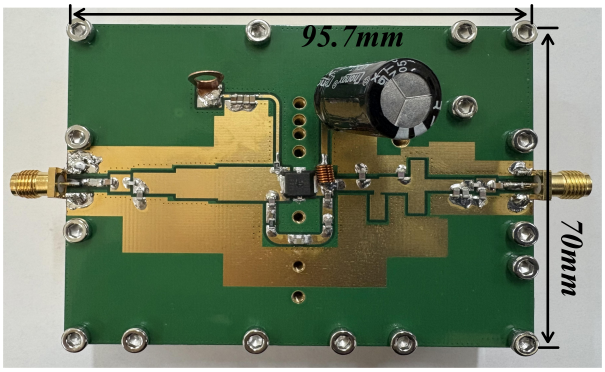

FIGURE 12. Photograph of fabricated PA.

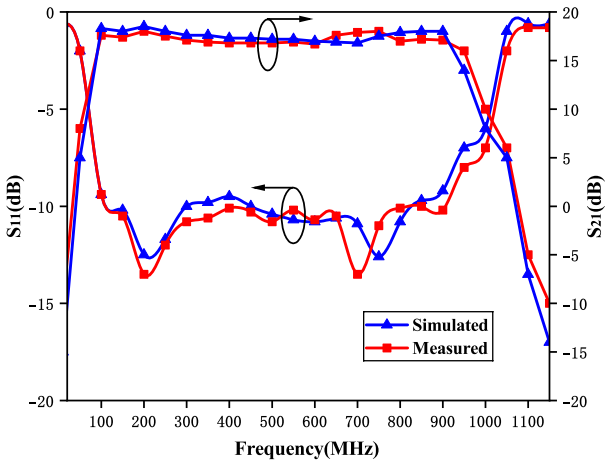

FIGURE 13. The simulated and measured S-parameters of the designed PA.

tures mature industrial processing technology and low fabrication costs, which significantly reduces device costs compared with Rogers series low-loss substrates. For the 100–900 MHz low-to-mid frequency band targeted in this design, the loss impact of the FR-4 substrate is far less pronounced than that in the high-frequency band, resulting in only slight drain efficiency degradation and gain loss relative to Rogers substrates. Such performance differences are entirely within the acceptable range for practical engineering applications, representing a reasonable trade-off that balances cost and utility. The physical dimensions of the heat sink for the designed power amplifier were determined as 95.7 mm × 70 mm to ensure good contact between the circuit board and the heat sink, thereby achieving excellent heat dissipation performance. In the layout design phase, it is crucial to ensure sufficient spacing between components and transmission lines to avoid unnecessary electromagnetic coupling and potential arc risks. A reasonable layout design plays an indispensable role in reducing spurious radiation, improving circuit isolation, and maintaining consistency between measured performance and simulated results. Fig. 12 shows the layout of the overall circuit.

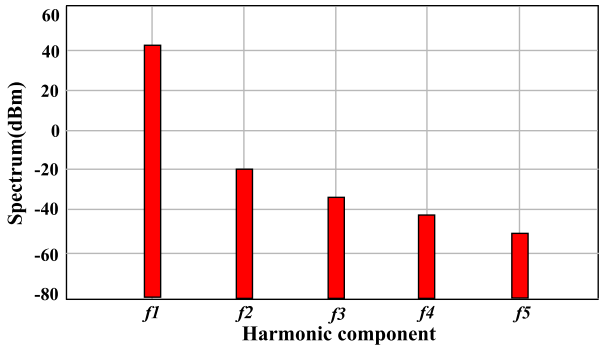

FIGURE 14. Frequency 400 MHz harmonic component.

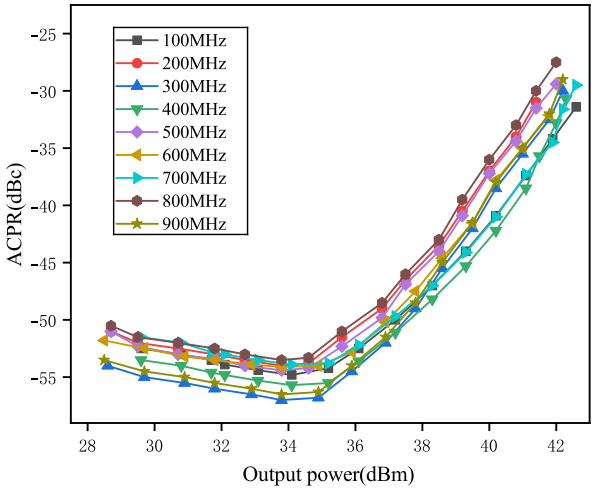

FIGURE 15. Measured ACPR versus output power across the 100–900 MHz band.

4.2. PA Simulation and Hardware Measurement

The simulated and experimental small-signal S-parameters of the power amplifier are presented in Fig. 13. The small-signal S-parameters were measured using a Rohde Schwarz ZNL6 vector network analyzer, with the measurement frequency range spanning from 50 to 1.5 GHz. The results demonstrate that S_{21} exhibits a gain of approximately 16.5–17.6 dB within the frequency band of 100–900 MHz, indicating favorable in-band gain flatness and high matching characteristics. Meanwhile, the measured S_{11} remains close to −10 dB across the operating band, satisfying the commonly accepted matching criterion for broadband RF power amplifiers. This matching level represents a practical trade-off among impedance matching, operating bandwidth, output power, drain efficiency, and circuit complexity. In addition, S_{21} decreases significantly, and S_{11} increases in the out-of-target bands, which signifies the effective suppression of out-of-band signals and verifies that the bandwidth is sufficient to meet the requirements of the target applications.

Meanwhile, the harmonic components of the output power spectrum are illustrated in Fig. 14. The measurement was performed at a fundamental frequency of 400 MHz with an input power of 25 dBm under saturated input conditions. The simulation results show that when the fundamental frequency is

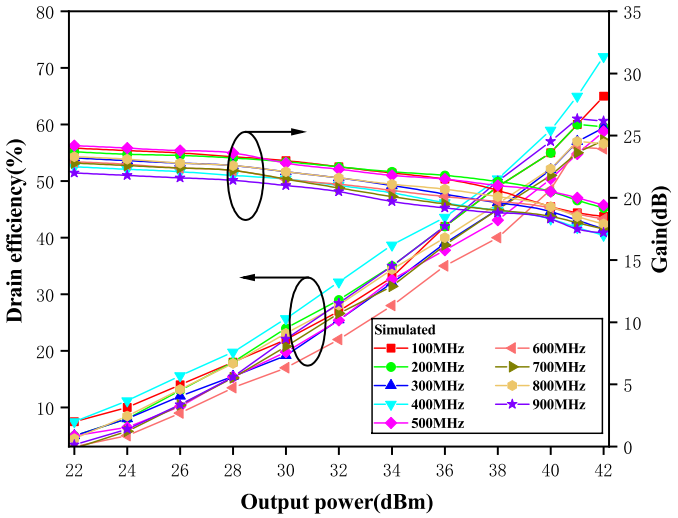

FIGURE 16. Simulated DE and gain versus Pout over 100–900 MHz.

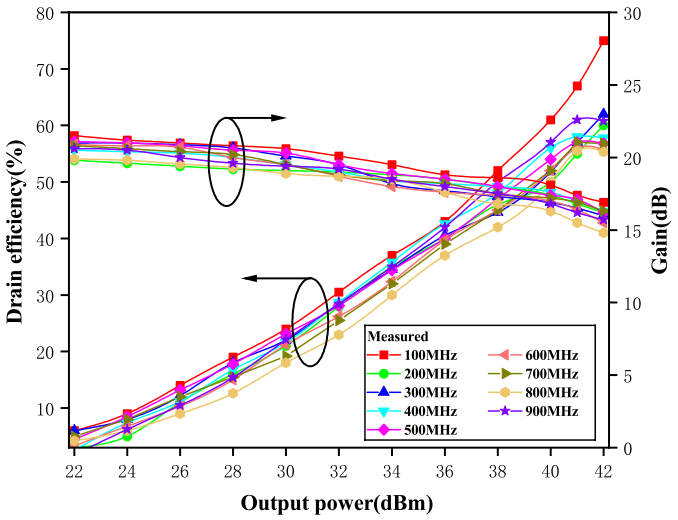

FIGURE 17. Measured DE and gain versus Pout over 100–900 MHz.

400 MHz, the fundamental power spectrum of the power amplifier reaches 41 dBm, whereas the second harmonic power spectrum component is only −20 dBm, corresponding to a harmonic suppression of 61 dBc. Fig. 15 shows the measured variation of adjacent channel power ratio (ACPR) with output power across the frequency band. Figs. 16 and 17 present the simulated and measured variations in drain efficiency and gain characteristics with output power. Differential evolution (DE) was obtained from the ratio of the measured RF Pout under continuous wave (CW) operation to the DC power consumption, with all tests performed under a 50 Ω load. On this basis, Fig. 18 shows the measured PAE versus output power across the 100–900 MHz band to fully analyze the efficiency characteristics of the amplifier at different output power levels and identify the high-efficiency operating region. Fig. 19 shows the simulated and measured curves of gain, output power, and efficiency corresponding to different frequencies under saturated input power conditions at each frequency point. The designed filtering power amplifier achieved excellent performance in the target frequency band of 100–900 MHz: the gain exceeded

TABLE 1. Performance comparison table of this design.

Ref.	Freq (GHz)	BW (GHz)	Psat (dBm)	Gain (dB)	Eff (%)
[6]	3.45–3.85	0.4	>38.5	MAX.12	MAX. 62.8 P
[16]	3.3–3.6	0.3	40.4–40.6	16	62.3–68.9 D
[18]	2.1–2.7	0.6	40.1	11.8	MAX. 69.8 P
[21]	0.7–1.3	0.6	38.4–41	>12	41–58 D
[22]	0.7–3.8	3.1	39–42.1	9–12.1	59–70 D
[23]	1.6–2.8	1.2	38–41	-	49–65 D
This work	0.1–0.9	0.8	40.5–42	16.5–17.6	55–75 D

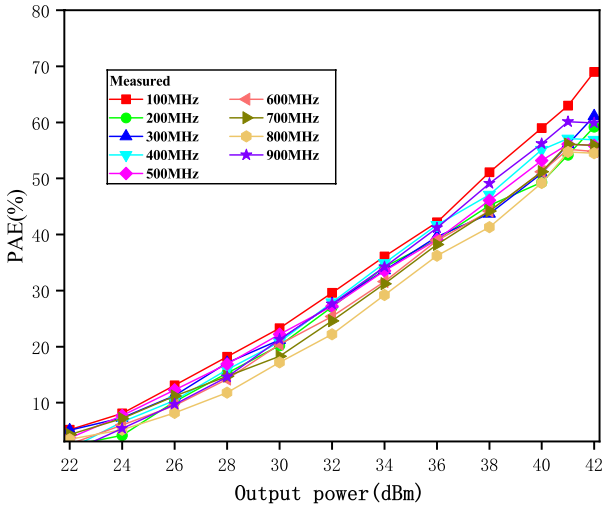

FIGURE 18. Measured PAE versus output power across the 100–900 MHz band.

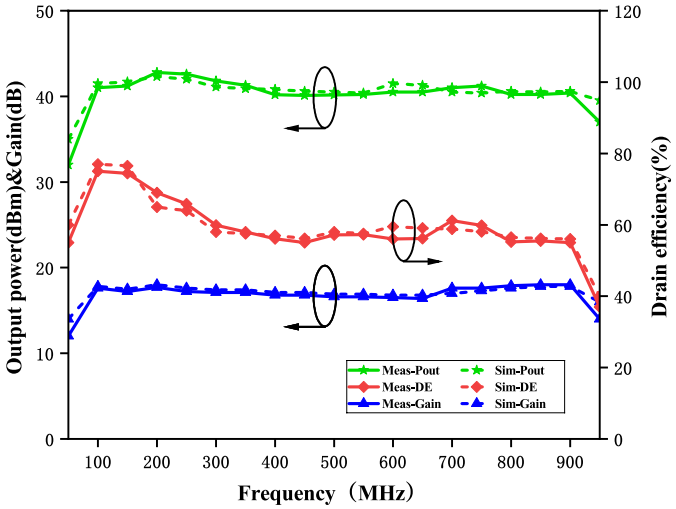

FIGURE 19. Curves of gain, power and efficiency at different frequencies (simulation vs. measurement).

16.5 dB; the drain efficiency was consistently maintained above 55%, with a peak drain efficiency of up to 75% under saturated operation; and the saturated output power ranged from 40.5 to 42 dBm. It can be observed from the measured curves that the actual performance of the circuit was slightly lower than that of the simulation.

This deviation is mainly caused by the combined effects of parasitic parameters, transmission loss, fabrication errors, and nonideal characteristics of the test link: FR-4 dielectric loss and microstrip radiation loss lead to signal attenuation; device parasitics and welding dimensional deviations reduce matching accuracy; test errors, impedance mismatch, and external electromagnetic interference also affect measurement results.

Despite discrepancies between the measured and simulated values caused by factors such as process fluctuations on the low-cost substrate, device parasitic effects, and test environment, the core performance trends (including the variation laws of S-parameters, efficiency, and gain with frequency and input power) show good consistency. This validates the feasibility and correctness of the proposed architectural design scheme.

Table 1 presents a comparative analysis of the performance of the proposed power amplifier and relevant state-of-the-art research results. The results demonstrate that, in contrast to other broadband power amplifier schemes, the proposed design features superior frequency selectivity, higher gain, and a wider operating bandwidth. Meanwhile, this power amplifier adopts a technical route integrating LDMOS transistors with FR-4 substrates. Compared with the mainstream GaN transistor-Rogers substrate solution, the proposed design features lower overall fabrication costs and higher process compatibility and delivers stable performance that meets the design requirements within the target frequency band.

5. CONCLUSION

This study proposes a broadband high-efficiency power amplifier that integrates both harmonic suppression and filtering characteristics. In the design process, Advanced Design System (ADS) software was employed to set the performance target parameters. To satisfy core requirements of broadband operation and high efficiency, the amplifier was integrated with band-pass filtering functionality by optimizing the topology of the impedance matching network. The simulation results demonstrate that the proposed amplifier operates over a frequency band spanning 100–900 MHz, with a saturated output power ranging from 40.5 to 42 dBm. The drain efficiency exceeds 55% across the entire frequency band, with a peak drain efficiency of up to 75% under saturated operation. The gain sta-

bilizes at 16.5–17.6 dB, corresponding to a relative bandwidth as high as 160%. In addition, the second harmonic suppression capability reached 61 dBc. This design not only achieves the development objectives of a broadband high-efficiency power amplifier but also successfully integrates the band-pass filtering functionality. The 100–900 MHz frequency band targeted in this design has engineering and practical application significance for current application requirements of low power consumption, wide coverage, and multi-scenario in communication systems. This verifies the remarkable advantages of the proposed network synthesis method in balancing bandwidth and efficiency, and its overall performance can fully meet broadband and high-efficiency application requirements of modern communication systems.

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