

Coordinated Control of Common Mode Voltage Suppression and Neutral Point Voltage Balance for NPC Three-Level Inverters

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ABSTRACT: To address high common-mode voltage (CMV) and neutral-point voltage (NPV) imbalance issues in practical neutral-point-clamped (NPC) three-level inverters, a logic virtual space vector pulse width modulation (LVSVPWM) strategy is proposed. Based on the conventional virtual space vector pulse width modulation (VSVPWM), the proposed method first eliminates vectors with large CMV and redivides small sectors to reduce sector switching, limiting the CMV to $\pm V_{dc}/6$. Second, it uses a logical judgment for the initial variable duty-cycle distribution to reduce the number of switching actions. Then, it redistributes the duty cycles according to NPV balancing requirements to achieve NPV balance. Finally, experiments validate the accuracy and effectiveness of the proposed strategy.

1. INTRODUCTION

Owing to their excellent harmonic characteristics, low voltage change rate, and low computational complexity, neutral-point-clamped (NPC) three-level inverters are widely adopted in electric drives and photovoltaic grid-connected systems [1]. However, when a permanent magnet synchronous motor is driven by it, an excessive amplitude of common-mode voltage (CMV) is introduced, which can cause motor bearing failure and electromagnetic interference, thereby affecting system reliability [2, 3]. Moreover, the neutral-point voltage (NPV) on the DC side exhibits drift, which degrades the output waveform quality and may damage components [4]. Therefore, suppressing CMV and balancing NPV have emerged as key control objectives for NPC inverters [5].

There are both hardware and software solutions to address CMV. Hardware solutions employ various common-mode filters, such as LRC filters, chokes, and transformers [6]; however, system costs increase. The software solution improves traditional modulation strategies by reducing the amplitude and hopping frequency of CMV in the time domain, or by suppressing specific harmonics in the frequency domain [7]. At present, most existing work on software solutions focuses on the time domain. In [8], a discontinuous pulse width modulation (DPWM) method is adopted to suppress CMV while reducing the number of switch actions, but the quality of the output waveform decreases. In [9], while suppressing CMV, a novel multisector modulation scheme is used to select switch sequences, reducing switch losses, but waveform distortion is severe. In [10], by adjusting the action time of a switching tube, the CMV is reduced; yet algorithm complexity is increased. In [11], an advanced model predictive control (MPC) method

based on discrete space-vector modulation is proposed, which fixes the switching frequency, but exacerbates waveform distortion. In [12, 13], the CMV can be effectively reduced by a simple algorithm; however, this advantage comes at the cost of additional hardware.

Although the above methods suppress CMV, the effect of NPV on CMV is ignored. To overcome this drawback, an improved time-sharing virtual space vector modulation strategy is proposed in [14], which achieves CMV suppression and NPV self-balancing but increases complexity and introduces additional current harmonics in the high-modulation index region. In [15], a new method is presented to simultaneously address NPV balance and CMV suppression, which can reduce the voltage change rate by 33% to 66% and limit the CMV amplitude to $V_{dc}/6$. However, the CMV spikes are still not eliminated. In [16], the principle of zero NPC outflow is proposed to redefine the medium vector and achieve NPV balance under all operating conditions. However, owing to the lack of feedback control, active balance cannot be achieved when the NPV drifts. In [17, 18], CMV suppression and NPV balance are achieved by optimizing virtual space vectors; however, NPV fluctuations are not eliminated. In [19], reconstructing virtual small and medium vectors effectively reduced the CMV and suppressed NPV oscillation over the full range. However, balancing the two objectives makes the design complex, and the performance heavily depends on specific parameters. In [20, 21], the coordinated control of CMV suppression and NPV balance is achieved by adding zero-sequence components, but the balancing effect is poor in the low-modulation region. In [22], the reconstruction of virtual small and medium vectors is employed to mitigate NPV drift; yet this approach's efficacy is constrained in the high-modulation range. In [23], full-

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range active adjustment of the NPV is achieved by optimizing the variable coefficients; however, the computational load is large. In [24], VSVPWM is applied to a ten-switch inverter to achieve simultaneous CMV suppression and NPV balancing, which verifies the versatility of the virtual vector method across different multilevel topologies to some extent but with increased harmonic content.

In summary, VSVPWM inherently involves many switching commutations. When a CMV suppression algorithm is incorporated, the computational burden is further increased, and the NPV balancing capability is degraded. To address these issues, a logic-based virtual space vector pulse width modulation (LVSVPWM) strategy is proposed in this study. By discarding vectors with higher CMV and dividing them into small sectors, logical operations are used to streamline vector selection, and the vector action time is allocated based on the NPV balance to achieve coordinated control of CMV suppression and NPV balance. The contributions of this study are as follows:

(1) By discarding high CMV vectors to suppress CMV, while reconstructing small sector partitioning and arranging the switching sequence reasonably, common mode spikes and sector misjudgments caused by vector and sector switching can be reduced.

(2) Based on CMV suppression, the proposed strategy simplifies vector selection through logical operations, eliminates the constraints of virtual vector pairs, and strengthens the correlation between vectors. While meeting the control requirements, the number of synthesized vectors is minimized as much as possible, thereby reducing the number of switching times. Simultaneously, by adjusting the vector action time based on NPV, the NPV's balance speed is improved, achieving collaborative control between the CMV and NPV.

The remainder of this paper is organized as follows. The causes of CMV and NPV imbalances are introduced in Section 2, and a coupling analysis of the two is conducted. In Section 3, the implementation principle of the traditional VSVPWM control strategy is analyzed, and its existing problems are identified. In Section 4, the LVSVPWM strategy is proposed, and a detailed analysis of the implementation steps is provided. The experimental results and analysis are presented in Section 5, followed by the conclusion.

2. ANALYSIS OF COMMON MODE VOLTAGE AND NEUTRAL POINT VOLTAGE OF NPC INVERTER

2.1. The Mechanism of CMV Generation

The topology of the NPC three-level three-phase inverter is illustrated in Fig. 1. The output voltage of the A-phase can be divided into $V_{dc}/2$, $-V_{dc}/2$, and 0, corresponding to levels P, N, and O, respectively, forming a total of 27 spatial voltage vectors, as shown in Fig. 2(a).

When the AC side of the inverter is externally connected to a motor, the CMV is defined as the potential difference between the motor NPV and the DC-bus NPV as follows:

$$U_{CMV} = \frac{1}{3}(U_a + U_b + U_c) \quad (1)$$

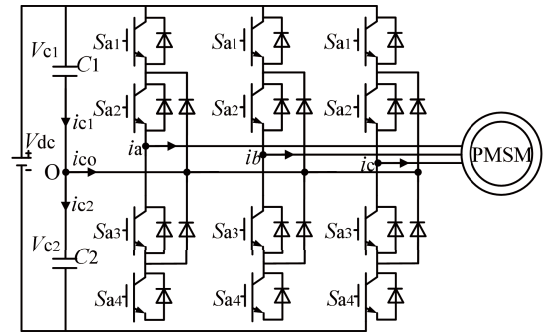


FIGURE 1. Topology of three-level NPC inverter.

where U_a , U_b , and U_c represent the phase voltages of inverters A, B, and C, respectively.

By substituting the switch function, the following expression is obtained:

$$U_{CMV} = \sum_{x=a,b,c} S_x \left(\frac{V_{dc}}{6} \right) \quad (2)$$

where V_{dc} is the DC bus voltage, and S_a , S_b , S_c are the switching states of three-phase bridge arms.

From (2), the switching state is directly related to CMV, and the NPC three-level can generate four types of CMV amplitudes: $\pm V_{dc}/2$, $\pm V_{dc}/3$, $\pm V_{dc}/6$, and 0.

2.2. The Mechanism of NPV Imbalance

When the switching state S_x of a certain phase bridge arm is "0", the neutral-point current flowing in or out charges and discharges capacitors C_1 and C_2 , causing fluctuations in NPV. The relationship between i_{np} and S_x is expressed as follows:

$$i_{np} = \left| \sum_{x=a,b,c} (1 - S_x) i_x \right| \quad (3)$$

where i_x represents the current of each phase, and i_{np} represents the neutral current.

To facilitate the expression of the degree of NPV balance, the offset Q of NPV is defined as:

$$Q = \frac{V_{dc1} - V_{dc2}}{V_{dc1} + V_{dc2}} \times 100\% \quad (4)$$

where V_{dc1} and V_{dc2} represent the voltages of capacitors C_1 and C_2 , respectively.

2.3. Coupling Analysis of CMV and NPV

When the minimum CMV modulation strategy is adopted in NPC inverters, the redundant small vectors originally used to balance the NPV are disabled, which disrupts the balance between action times of the positive and negative small vectors, resulting in significant oscillations of the NPV in the low-frequency range. Therefore, suppressing the CMV often comes at the expense of the NPV balancing capability.

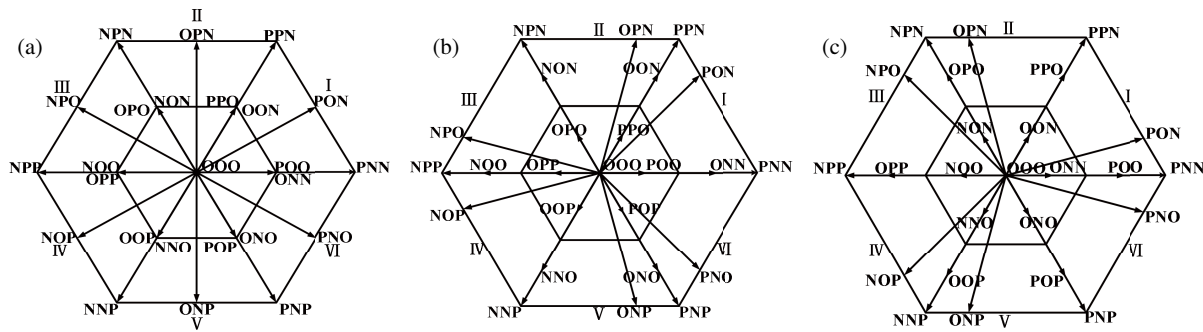


FIGURE 2. Space vector diagram of 3L-NPC converter (a) $Q = 0$, (b) $Q < 0$, (c) $Q > 0$.

TABLE 1. Coupling analysis of all vector NPV and CMV in three-level inverter.

Vector type	Space vector	i_{np}	$ CMV $	Synergistic effect
Zero vector	OOO	0	0	Ideal choice
	PPP NNN	0	$V_{dc}/2 + Q * V_{dc}/2$	High CMV
Small vector	POO OON OPO	Adjustable (P/N type)	$V_{dc}/6 + Q * V_{dc}/6$	Proactively balancing NPV
	NOO OOP ONO			
	ONN PPO NON	Adjustable (P/N type)	$V_{dc}/3 + Q * V_{dc}/3$	Higher CMV
	OPP NNO POP			
Medium vector	PON OPN NPO NOP ONP PNO	fixed	$ Q * V_{dc}/3$	Suppressing CMV but mitigating NPV fluctuations
Large vector	PNN PPN NPN NPP NNP PNP	0	$V_{dc}/6 + Q * V_{dc}/2$	Higher CMV

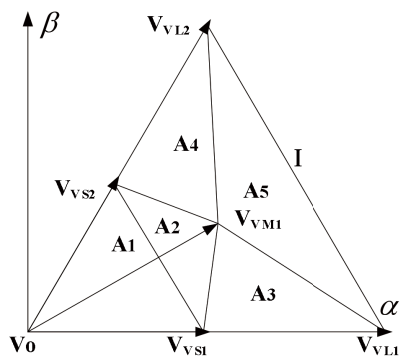


FIGURE 3. Vector diagram of VSPWM in sector I.

When an NPV deviation occurs, the voltage borne by the switching tubes of the upper and lower bridge arms is inconsistent with $V_{dc}/2 - \Delta V$ and $V_{dc}/2 + \Delta V$, respectively, causing changes in the output phase voltage and amplitude or direction of some vectors, and introducing additional even-order harmonics, which are directly superimposed on the CMV waveform, as shown in Figs. 2(b) and (c). In motor drive systems, the coupling effect further exacerbates the risk of shaft voltage and bearing electrical corrosion. Therefore, while effectively inhibiting CMV, it is necessary to suppress the NPV imbalance.

According to (2) and (3), the relationship between CMV and NPV is shown in Table 1. From Table 1, suppressing CMV requires the use of a zero-vector OOO and a medium vector with

zero CMV. However, the medium vector lacks paired vectors, which cannot balance the NPV and instead exacerbate its fluctuations. Meanwhile, discarding vectors with larger CMV results in the inability of positive and negative small vectors to appear in pairs, making it difficult to achieve NPV balance.

3. TRADITION VSPWM CONTROL STRATEGY

In traditional VSPWM, the average current flowing into the neutral point is adjusted by changing variable coefficients of the virtual medium and small vectors, thereby achieving NPV balance. Taking the first largest sector as an example, sector I is divided into five small sectors, A_1 – A_5 , by the lines connecting virtual small vectors, the virtual medium vectors, and the virtual large vectors, as shown in Fig. 3. In Fig. 3, V_{V0} is the virtual zero vector; V_{VS1} and V_{VS2} are the virtual small vectors; V_{VM1} is the medium vector; and V_{VL1} and V_{VL2} are the virtual large vectors.

The expressions for each virtual vector are as follows:

$$\begin{cases} V_{V0} = V_{OOO} \\ V_{VL1} = V_{PNN} \\ V_{VL2} = V_{PPN} \\ V_{VS1} = \frac{1}{2}K_1 V_{ONN} + \frac{1}{2}(1 - K_1)V_{POO} \\ V_{VS2} = \frac{1}{2}K_2 V_{PPO} + \frac{1}{2}(1 - K_2)V_{OON} \\ V_{VM1} = K_3 V_{PON} + \frac{1}{2}(1 - K_3)V_{PPO} + \frac{1}{2}(1 - K_3)V_{ONN} \end{cases} \quad (5)$$

where k_1 , k_2 , and k_3 are variable coefficients that satisfy $0 < k_1 < 1$, $0 < k_2 < 1$, and $0 < k_3 < 1$.

According to (5), in the traditional VSPWM strategy, when the virtual space vectors are synthesized, small vectors with larger CMV, such as ONN and PPO, are introduced, resulting in a maximum CMV of $V_{dc}/3$. Moreover, the combination of virtual vectors is fixed and composed of multiple basic vectors, leading to higher switching losses.

Owing to the system's three-phase symmetry, the current balance expression is as follows:

$$i_a + i_b + i_c = 0 \quad (6)$$

where i_a , i_b , and i_c represent the currents of phases A, B, and C, respectively.

Taking the virtual medium vector as an example, in VSPWM, the NPV is balanced by adjusting its k_3 value. According to (6), the average neutral point current can be expressed as:

$$i_M = (2K_3 - 1)i_b \quad (7)$$

where i_M is the neutral point current of the virtual medium vector.

From (7) and (5), by constraining the action time of the basic vectors PPO and ONN to be equal, the neutral-point currents of the basic vectors PPO and ONN and vector PON are equal in magnitude and opposite in direction. By changing k_3 and adjusting the magnitude and direction of i_M , an NPV balance can be achieved. The essence of this method is to balance the NPV by controlling the current of a certain phase; however, the flexibility of allocating the basic vector action time is limited.

A coordinated control method for CMV suppression and NPV balance based on LVSPWM is proposed to address the shortcomings of traditional VSPWM control strategies.

4. LVSPWM CONTROL STRATEGY

4.1. Design of CMV Suppression

As shown in Fig. 3, in the traditional VSPWM, the division of small sectors is complex, and the CMV is relatively large. When the virtual medium vector coefficient k_3 is $1/3$, after mapping its basic vector to sector II, there are four values for the vertical axis: 0 , $\sqrt{3}V_{dc}/6$, $2\sqrt{3}V_{dc}/9$, $\sqrt{3}V_{dc}/3$. However, the proposed LVSPWM method uses four values of the vertical axis to redivide the small sectors. To simplify the analysis, the re-partitioned vector of sector I is mapped to sector II through coordinate transformation, as shown in Fig. 4.

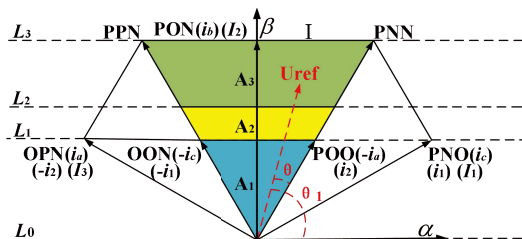


FIGURE 4. Vector diagram mapping from sector I to sector II in LVSPWM strategy.

In the LVSPWM method, the selection and sorting principles of switch states are as follows:

- (1) Low CMV switch states are used as much as possible.
- (2) The switching states are arranged reasonably. To prevent short circuits in power devices, the same bridge arm cannot switch directly between the N and P states.
- (3) The switching sequence satisfies the central symmetry.
- (4) To reduce the fluctuation of NPV, the fundamental vectors that affect NPV within a control cycle must contain two or more vectors, and the effects must be opposite.

As shown in Fig. 4, the first sector is divided into three areas, A_1 , A_2 , and A_3 by L_1 , L_2 , and L_3 . L_1 is the line connecting PPO and OON, L_2 is the horizontal line perpendicular to the end of the virtual medium vector with $K_3 = 1/3$, and L_3 is the line connecting PNN and PPN. L_1 , L_2 , and L_3 are represented as

$$\begin{cases} L_0 : y = 0 \\ L_1 : y - \frac{\sqrt{3}}{6}V_{dc} = 0 \\ L_2 : y - \frac{2\sqrt{3}}{9}V_{dc} = 0 \\ L_3 : y - \frac{\sqrt{3}}{3}V_{dc} = 0 \end{cases} \quad (8)$$

where y denotes the ordinate in the α - β coordinate system.

As shown in Fig. 4, the basic vectors of each small sector have only two heights; that is, each reference vector can be synthesized from a virtual upper-layer vector and a virtual lower-layer vector. Therefore, new virtual vectors are defined as:

$$\begin{cases} A_1 : \begin{cases} V_{VSU} = d_1PNO + d_2POO + d_4OON + d_5OPN \\ V_{VSD} = OOO \end{cases} \\ A_2 : \begin{cases} V_{VSU} = PON \\ V_{VSD} = d_1PNO + d_2POO + d_4OON + d_5OPN \end{cases} \\ A_3 : \begin{cases} V_{VSU} = d_2PNN + d_3PON + d_4PPN \\ V_{VSD} = d_1PNO + d_5OPN \end{cases} \end{cases} \quad (9)$$

where V_{VSU} and V_{VSD} denote the virtual upper- and lower-layer vectors, respectively, and $d_1 \sim d_5$ are variable duty cycle coefficients, satisfying $0 < d < 1$.

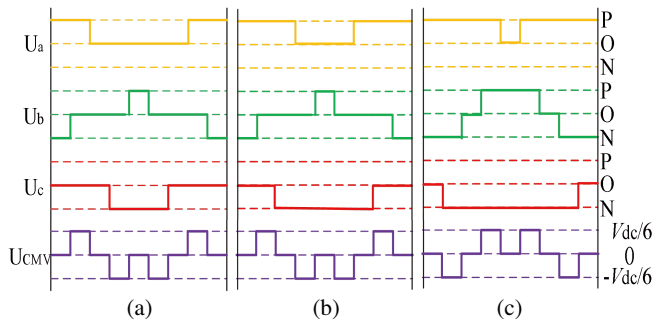
To overcome the inflexible allocation of basic vector action time and the high number of switch actions in the traditional VSPWM, combined with selection and sorting principles of the LVSPWM switch states, the basic vectors and their sorting for each small sector action are designed, as shown in Table 2.

According to Table 2, the switching state sequences and CMV waveforms of each phase in A_1 – A_3 are shown in Figs. 5(a)–(c). Owing to the removal of the larger CMV vectors, the amplitude of CMV is suppressed to $\pm V_{dc}/6$. To avoid significant jumps in CMV, the switching sequence is arranged reasonably, with both the starting and ending vectors being medium vectors, thereby reducing CMV jumps caused by sector switching, suppressing CMV spikes, and minimizing electromagnetic interference.

L_1 , L_2 , and L_3 reduce the number of small sectors from A_1 – A_5 in Fig. 3 to A_1 – A_3 in Fig. 4, which not only decreases the number of small sectors, but also reduces the number of reference vector switches between different small sectors, as

TABLE 2. Sequence of voltage vector action in sector I.

Small sectors	Basic vector	Vector sequence
A1	OOO-PNO-POO-OPN-OPN	PNO-POO-OOO-OPN-OPN-OPN-OPN-POO-PNO
A2	PNO-POO-OPN-OPN-OPN	PNO-POO-PON-OPN-OPN-OPN-OPN-POO-PNO
A3	PNO-PNN-PON-PPN-OPN	PNO-PNN-PON-PPN-OPN-PPN-PON-PNN-PNO

**FIGURE 5.** The sequence of switch states for each phase in A1–A3.

shown in Fig. 6. It is switched only three times in the middle-modulation region, and there is no switching in the low- and high-modulation regions, which weakens adverse effects such as increased harmonic content, zero-crossing distortion, and enhanced electromagnetic interference caused by cross-cycle sector switching.

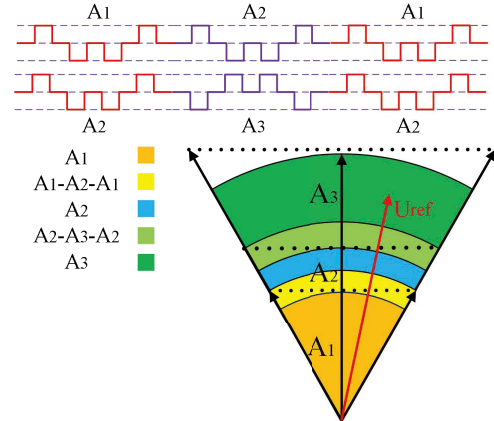
In traditional VSVPWM, only three virtual vectors are used to synthesize the reference vector within each. Based on the principle of the nearest three vectors, the action time of each virtual vector can be obtained by solving the three equations. However, when only two virtual vectors are involved, the LVSVPWM strategy designed for CMV suppression is no longer suitable for the nearest three-vector principle. Meanwhile, owing to the abandonment of larger CMV vectors, positive and negative small vectors cannot appear in pairs, making it difficult to achieve NPV balance. To address these issues, an NPV balance control method is proposed.

4.2. Design of NPV Balance

Based on the CMV suppression design, the variable duty cycle of the virtual vectors is initially allocated according to the principle of minimum vector combination for the proposed LVSVPWM method. Then, based on the NPV balance requirements, the variable duty cycle is redistributed to determine the action time of the five different vectors, achieving coordinated control of the CMV and NPV balance.

4.2.1. NPV Balance in Small Sectors A₁ and A₂

For LVSVPWM, the NPV balancing method is consistent in small sectors A₁ and A₂, using A₂ small sector as an example. When the reference voltage vector U_{ref} is located in the A₂ region, its control steps are divided into the initial allocation and redistribution of variable duty cycles.

**FIGURE 6.** Small sector switching diagram of reference vector.

Taking the medium vector as a reference, the modulation index M is defined as follows:

$$M = \frac{\sqrt{3}|U_{ref}|}{V_{dc}} \quad (10)$$

where U_{ref} is the reference vector.

(1) Initial allocation of variable duty cycles

From horizontal and vertical components of the reference vector, x and y are obtained as follows:

$$\begin{cases} y = U_{ref} \sin \theta_1 \\ x = U_{ref} \cos \theta_1 \end{cases} \quad (11)$$

where x and y are the horizontal and vertical components of the reference vector, respectively, and $\theta_1 = \theta + \pi/3$.

As shown in Fig. 4, all the basic vectors have only three heights. Because the small sectors are divided by horizontal lines, the basic vector of each small sector has only two heights, defined as the upper and lower heights, respectively. According to (8), the heights of the upper and lower layers in area A₂ are $2\sqrt{3}V_{dc}/9$ and $\sqrt{3}V_{dc}/6$, respectively.

From (9) and Fig. 4, the vertical axis of the virtual vector composed of multiple vectors is constant. Based on the proportional relationship between the y -value and the heights of the upper and lower layers, D_U and D_D are obtained as follows:

$$\begin{cases} D_U = \frac{y - \frac{\sqrt{3}}{6} V_{dc}}{\frac{\sqrt{3}}{6} V_{dc}} \\ D_D = 1 - D_U \end{cases} \quad (12)$$

where D_U and D_D are the duty cycles of the virtual upper- and lower-layer vectors, respectively.

In region A2, only one vector (PON) acts on the virtual upper layer. Let the duty cycle of PON be d_3 , then $d_3 = D_U$. Given that the x -coordinate of the PNO is zero, the virtual lower-layer vector D_2 can be derived by establishing a volt-second balance equation for the outer vectors of the virtual lower layer based solely on the x -component of the reference vector. The expression is as follows:

$$D_2 = \frac{\frac{2x}{D_D V_{dc}} + 1}{2} \quad (13)$$

where D_2 represents the variable duty cycle of the right vector PNO when the virtual lower vector is composed solely of the two vectors PNO and OPN. The duty cycle satisfies $0 \leq D_2 \leq 1$.

d_1 and d_2 can be represented by D_2 as follows:

$$\begin{cases} d_1 = D_2 \\ d_5 = (1 - D_2) \end{cases} \quad (14)$$

Unlike the VSPWM method, LVSVPWM does not rely on fixed virtual vector constraints. Instead, the NPV balance is achieved through an equivalent vector transformation. The four transformations are as follows:

$$\begin{cases} \text{PNO} + \text{OPN} = \text{OON} + \text{POO} \\ 2\text{POO} = \text{PNO} + \text{OON} \\ 2\text{OON} = \text{POO} + \text{OPN} \\ 2\text{PON} = \text{PNN} + \text{PPN} \end{cases} \quad (15)$$

According to (15), the equivalent transformation of PNO and OPN can be obtained as follows:

$$\begin{cases} d = \min(d_1, d_5) \\ d_1 = d_1 - d \\ d_2 = d \\ d_4 = d \\ d_5 = d_5 - d \end{cases} \quad (16)$$

Similarly, based on (16), the virtual lower-layer vectors are equivalently transformed according to (15). According to the nearest three-vector principle, when $x > 1/6V_{dc}$, $|x| \leq 1/6V_{dc}$, and $x < -1/6V_{dc}$, the final transformations yield three combinations: (PNO, POO), (POO, OON), and (OON, OPN). In each case, only two basic vectors participate in the synthesis, which constitutes the initial allocation.

(2) Reassignment of variable duty cycles

The initial allocation has already established the variable duty cycle of the virtual vector based on the vertical component. The horizontal component of the virtual vector is now obtained from the NPV balance to achieve a second redistribution of the variable duty cycle.

The virtual upper vector participating in synthesis is solely PON, which requires no further duty-cycle reassignment. In contrast, the virtual lower vector comprises four active vectors: PNO, POO, ONN, and OPN, whose neutral-point currents directly influence the NPV. The neutral-point currents generated

by PNO, POO, ONN, and OPN are i_c , $-i_a$, $-i_c$, and i_a , respectively. Thus, i_c and $-i_c$, as well as i_a and $-i_a$, have opposite effects on the NPV, which facilitates subsequent assignment and decision logic. Define i_1 as the neutral-point current i_c produced by PNO, and i_2 as the neutral-point current $-i_a$ produced by POO, as shown in Fig. 4.

Within a single control cycle, based on the magnitude of the NPV offset Q , the neutral-point current required for NPV balancing is given as follows:

$$i_{co} = -\frac{CV_{dc}Q}{T_s} \quad (17)$$

where i_{co} is the neutral-point current required for NPV balancing when there is no initial duty-cycle distribution.

After the initial distribution, the variable duty cycle that needs to be adjusted for NPV balancing with the virtual lower-layer vectors is given by:

$$\begin{cases} i'_{co} = \frac{(i_{co} - D_D(d_1 i_1 + d_2 i_2 - d_4 i_1 - d_5 i_2) - D_U i_3)}{D_D} \\ d = \frac{i'_{co}}{i} \end{cases} \quad (18)$$

where i'_{co} is the lower-layer vector neutral-point current required for NPV balancing after the initial distribution, and i is the varied midpoint current after vector adjustment.

If variable duty-cycle adjustment is performed via equivalent transformation $\text{POO} + \text{OPN} = 2\text{OON}$, the duty cycles are redistributed with d from (18) as $d_2 - d/2$, $d_5 - d/2$, and $d_4 + d$, giving adjusted current $i = -i_c$.

The steps for redistributing the duty cycle are as follows:

Step 1: Determine the initial combination of virtual lower vectors by evaluating the range of x .

Step 2: Assess whether i_1 and i_2 have the same sign to establish the relative direction of the neutral point currents for each vector within the virtual lower vector set.

Step 3: Determine the influence of each virtual lower vector on the NPV balance by checking whether i_1 and i'_{co} have the same sign, thereby enabling the allocation of variable duty cycles to the virtual lower vectors.

Based on the aforementioned steps for the second redistribution of the duty cycle, there exist twelve possible cases, each of which follows a broadly similar resolution approach. The following two representative cases are illustrated as examples.

Case 1:

1) First, determine the range of x . $|x| \leq 1/6V_{dc}$, the initial virtual lower vectors are POO and OON.

2) Next, assess whether i_1 and i_2 have the same sign. If not, the contributions of POO (i_2) and OON ($-i_1$) to NPV are identical. Based on the relationship between the vector neutral-point currents of the vectors, POO (i_2) and OON ($-i_1$) exert opposing effects on the NPV compared to OPN ($-i_2$) and PNO (i_1).

3) Finally, determine whether i_1 and i'_{co} have the same sign. If so, based on the initial allocation, the virtual lower vectors are POO and OON. Combined with the previous two judgments, POO and OON are detrimental to NPV balance, and their variable duty cycles must be reduced to achieve the NPV balance.

To minimize switching actions, it is necessary to check whether the variable duty cycle of $\max(|d_2 \times i_2|, |d_1 \times i_1|)$ satisfies (18) for NPV balance. If satisfied, perform an equivalent transformation according to (15). Assuming that $|d_2 \times i_2|$ is larger, part of POO is transformed into PNO and OON, i.e., $d_2 - d$, $d_1 + d/2$, $d_4 + d/2$. After redistribution, the duty cycle of OPN remains zero, thereby reducing switching actions. If not satisfied, part of the POO and OON is transformed into PNO and OPN, achieving maximum NPV balance while still synthesizing the target vector.

Case 2:

1) First, determine the range of x . If $x > 1/6V_{dc}$, the initial virtual lower vectors are PNO and POO.

2) Next, assess whether i_1 and i_2 have the same sign. If so, POO (i_2) and PNO (i_1) have the opposite effect on the NPV compared to OON ($-i_1$) and OPN ($-i_2$).

3) Finally, determine whether i_1 and i'_{co} have the same sign. If not, according to the initial allocation, the virtual lower vectors are PNO and POO. Within region A2, it can be concluded that $d_2 \geq 5 \times d_1$ indicates that the action time of POO is longer than that of PNO. Therefore, when NPV is in equilibrium, POO dominates. To reduce switching actions, according to (15) and (18), only POO is converted into PNO and OON.

The other cases follow the same reasoning.

As shown in Table 2, both the LVSVPWM and conventional VSPWM strategies adopt nine-segment modulation. In sector A2, LVSVPWM uses logical judgment for the initial and redistribution of duty cycles, leading to $d_1 = 0$ or $d_5 = 0$: PON or OPN does not participate in vector synthesis, reducing the number of switching actions.

4.2.2. Balance of NPV in A₃ Small Sector

When the reference vector U_{ref} is located in region A3, its control procedure also includes the initial and redistribution of variable duty cycles. The outer vector of the virtual vector is represented only by the transverse component of the reference vector, and the volt-second balance equation is derived as follows:

$$\frac{D_U(2D_1 - 1)V_{dc}}{3} + \frac{D_D(2D_2 - 1)V_{dc}}{2} = x \quad (19)$$

According to (19) and the constraint $0 \leq D_2 \leq 1$, the range of D_2 is obtained. The maximum and minimum values of D_2 are denoted as D_{2max} and D_{2min} , respectively.

As shown in Fig. 4, only the PON vector in the virtual upper vector affects the NPV, with the neutral-point current being I_2 . The virtual lower vector consists of PNO and OPN, with neutral-point currents I_1 and I_3 , respectively. Balancing NPV first with virtual lower-layer vectors gives D'_2 :

$$D'_2 = \frac{\frac{i_{co}-I_2}{D_D} - I_3}{I_1 - I_3} \quad (20)$$

where D'_2 denotes the duty cycle needed for NPV balancing.

(1) Initial Distribution of Variable Duty Cycles

When the reference voltage vector U_{ref} is located in region A3, the specific steps for the initial duty cycle distribution are as follows:

Step 1: Judge whether I_2 and i_{co} have the same sign to determine whether the virtual lower-layer vectors provide over-compensation or under-compensation for the NPV balance.

Step 2: Check whether D'_2 falls within the value range of D_2 , then complete the initial distribution of d_1 , d_2 , d_4 , and d_5 .

To avoid over-compensation of the neutral-point current, the compensation coefficient E is defined as:

$$E = \frac{[D_2(I_1 - I_3) + I_3] D_D}{i_{co}} \quad (21)$$

where $E < 1$ indicates under-compensation, and $E > 1$ indicates over-compensation.

After the initial distribution, the variable duty cycles d_1 , d_2 , d_4 , and d_5 are given as:

$$\begin{cases} d_1 = D_2 \\ d_2 = D_1 \\ d_4 = (1 - D_1) \\ d_5 = (1 - D_2) \end{cases} \quad (22)$$

In the above redistribution steps, two redistribution modes exist: under- and over-compensation.

Case 1: Under-compensation

1) First, determine whether I_2 and i_{co} have the same sign. If $I_2 \times i_{co} > 0$, the under-compensation mode is adopted.

2) Then, check whether D'_2 falls within the range of D_2 . If yes, set $D_2 = D'_2/2$, and the remaining NPV deviation is balanced by vector PON with the current I_2 . Otherwise, substitute $D_2 = D_{2max}$ and $D_2 = D_{2min}$ into (21), and select the value closest to 1 as the final D_2 . A minimum action time is set for the PON to avoid large jumps in the CMV.

Case 2: Over-compensation

1) First, check whether I_2 and i_{co} have the same sign. If $I_2 \times i_{co} < 0$, the over-compensation mode is adopted.

2) Then, check whether D'_2 falls within the range of D_2 . If yes, set $D_2 = D_{2max}$ and $D_2 = D_{2min}$ into (21), and select the value that satisfies $E > 1$ as the final D_2 (If $E > 1.5$, clamp E to 1.5 and take the corresponding D_2 . At this moment, D_2 should not be too large or too small to prevent d_3 from being insufficient for NPV balancing after redistribution, which causes reverse over-regulation). If D'_2 is outside the range of D_2 , set $D_2 = D_{2max}$ when $D'_2 > D_{2max}$; otherwise set $D_2 = D_{2min}$.

(2) Redistribution of variable duty cycles

From the NPV balancing requirement, the redistributed d_3 is given as:

$$d_3 = \frac{i_{co} - D_D(D_2(I_1 - I_3) + I_3)}{D_U I_2} \quad (23)$$

According to (23), the duty cycle d_3 required for NPV balancing can be obtained. Subsequently, d_2 , d_3 , and d_4 are redistributed based on (9) and the constraints on the variable duty

cycle, thereby determining the variable duty cycles of the virtual vectors.

In region A3, LVSVPWM employs logical judgment for the initial and redistribution of duty cycles, where D_2 may take values of 0 or 1, reducing the number of switching actions. The logic flow of the LVSVPWM is illustrated in Fig. 7.

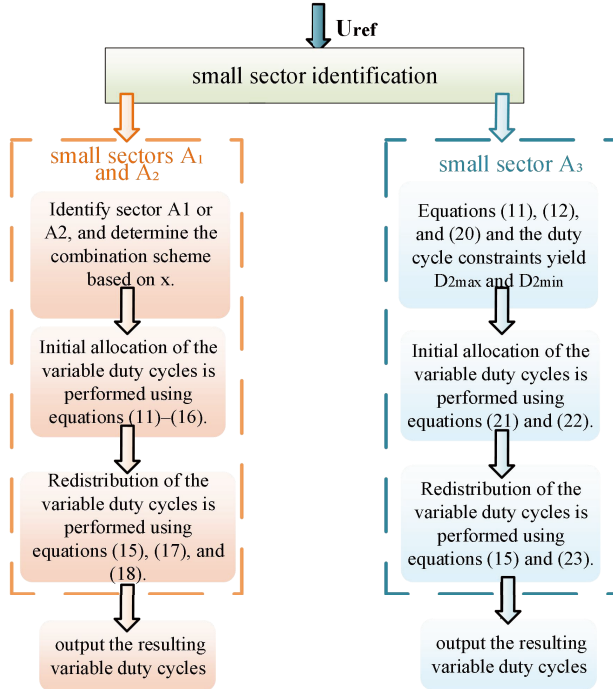


FIGURE 7. Control flowchart of the LVSVPWM strategy.

The system block diagram of the proposed LVSVPWM strategy is shown in Fig. 8.

5. EXPERIMENTAL RESULTS AND ANALYSIS

To verify the correctness of the proposed method, an RT-LAB experimental platform is used to compare STV-MPCC and ERSTV-MPCC with traditional TV-MPCC methods. The experimental platform is shown in Fig. 9.

The DC-link voltage of the inverter is obtained by rectifying the grid voltage via the rectifier, with $V_{dc} = 800$ V, a control frequency of 10 kHz, capacitance of 5600 μ F, and dead time of 1.5 μ s. The motor parameters are listed in Table 3.

Figure 10 shows the experimental results of VSPWM, IVSVPWM, and the proposed LVSVPWM strategies at 800 r/min and 30 N·m load torque, where V_{AB} , i_a , V_{CMV} , and ΔV_{np} denote line voltage, phase-A current, CMV, and DC-bus capacitor voltage error, respectively. As shown in Fig. 10, V_{CMV} of conventional VSPWM is about ± 267 V ($\pm V_{dc}/3$), whereas that of the proposed LVSVPWM and IVSVPWM is only ± 133 V ($\pm V_{dc}/6$). IVSVPWM and LVSVPWM achieve similar NPV control performance, both having a ΔV_{np} of 11.2 V, whereas VSPWM exhibits a larger fluctuation of 14.6 V.

As shown in Fig. 11, at 1800 r/min and 30 N·m, VSPWM, IVSVPWM, and the proposed LVSVPWM have similar ΔV_{np}

TABLE 3. Motor parameters.

Parameters	Value
DC-link voltage (V)	800
Rated speed n (r/min)	2000
Rated current I (A) stator	40
Rated torque (N·m)	50
L_d (H)	5.2e-3
L_q (H)	12e-3
Stator resistance R (Ω)	0.958
Polar logarithmic p	4
Moment of inertia J (10^{-4})	0.003

of approximately 15.4 V. NPV fluctuation increases with rising load. At 47 N·m, VSPWM and the proposed LVSVPWM still exhibit comparable NPV control performance, both with a ΔV_{np} of about 20.6 V, whereas IVSVPWM shows a smaller fluctuation of about 18.8 V. Combined with Fig. 10, it can be concluded that over the entire modulation range, VSPWM has no CMV suppression capability, with CMV stabilized at approximately ± 267 V ($\pm V_{dc}/3$), whereas both IVSVPWM and the proposed LVSVPWM can maintain CMV at ± 133 V ($\pm V_{dc}/6$) over the full range. Among them, IVSVPWM achieves the smallest NPV fluctuation, followed by LVSVPWM, and VSPWM exhibits the largest.

As shown in Fig. 12, with a 100 V voltage difference between the upper and lower capacitors in the low-modulation region ($M = 0.3$), the NPV settling times of VSPWM, IVSVPWM, and the proposed LVSVPWM are 0.08 s, 0.13 s, and 0.12 s, respectively. In terms of NPV balancing speed, VSPWM is the fastest, followed by LVSVPWM, and IVSVPWM is the slowest.

As shown in Fig. 13, with a 100 V voltage difference between the upper and lower capacitors, in the medium-modulation region ($M = 0.65$), the NPV settling times of VSPWM, IVSVPWM, and the proposed LVSVPWM are 0.13 s, 0.14 s, and 0.09 s, respectively, while in the high-modulation region ($M = 0.9$), they are 0.08 s, 0.08 s, and 0.06 s, respectively. Combining Figs. 12 and 13, LVSVPWM is slightly inferior to VSPWM but superior to IVSVPWM in NPV regulation capability in the low-modulation region, and it outperforms both in the medium- and high-modulation regions.

As shown in Fig. 12, at low modulation ($M = 0.3$), the reference voltage vector has a small magnitude, which limits the available effective vectors and shortens the dwell time of redundant small vectors used for NPV regulation, thereby reducing the control gain. Furthermore, the proposed strategy intentionally excludes certain redundant vectors with high CMV to prioritize CMV suppression, further limiting the degree of freedom for NPV balancing. This accounts for the slower dynamic response than traditional VSPWM, reflecting an inherent trade-off between CMV suppression and NPV balancing. Nevertheless, the settling time of 0.12 s remains acceptable for most low-modulation operating conditions, and the proposed method outperforms VSPWM in terms of settling speed in the medium- and high-modulation regions.

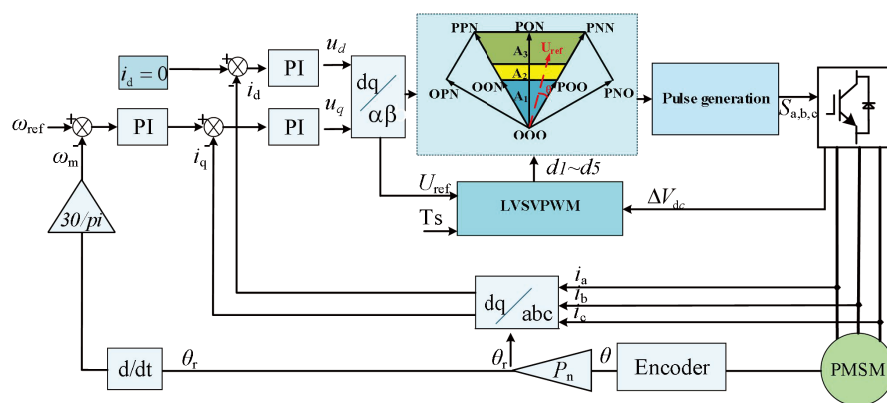


FIGURE 8. System block diagram of the proposed LVSVPWM strategy.

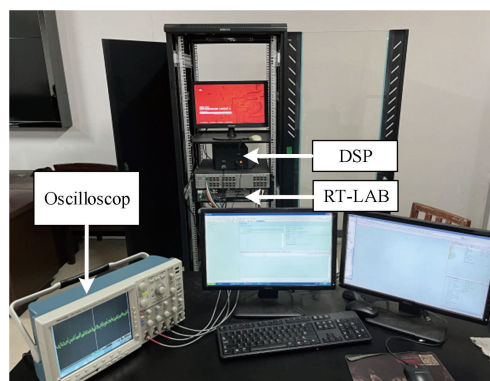


FIGURE 9. RT-LAB platform.

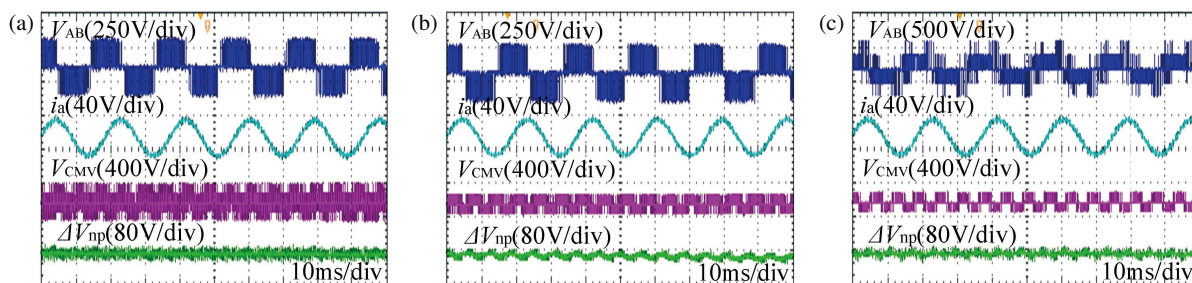


FIGURE 10. Steady-state experimental results at 800 r/min and 30 N·m. (a) VSVPWM, $M = 0.3$, (b) IVSVPWM, $M = 0.3$, and (c) LVSVPWM, $M = 0.3$.

Table 4 presents the total harmonic distortion (THD) values of different methods under various modulation indices. Since only low-CMV vectors are adopted and the vector span is expanded, the THD of i_a and V_{AB} for LVSVPWM and IVSVPWM is slightly higher than that of VSVPWM. Nevertheless, LVSVPWM achieves a lower 7th harmonic content. Particularly in the high-modulation region, the 5th and 7th harmonic contents of the proposed strategy are smaller than those of VSVPWM and IVSVPWM, which effectively suppresses motor torque ripples. Although the i_a THD of LVSVPWM is marginally higher than that of IVSVPWM in the low-modulation region, it becomes lower under medium and high modulation ratios.

Based on the data in Table 4, compared with VSPWM, the additional copper loss caused by the higher phase current THD is estimated at 2%–4% of the rated copper loss, corresponding to a temperature rise of approximately 2–3°C. The line voltage harmonics contribute an extra iron loss of about 5%–10% in the low-modulation region and about 3%–5% in the medium-modulation region, leading to a core temperature increase of 1–2°C. The total temperature rise (≈ 3 –5°C) remains well below the permissible limits for Class B/F insulation.

It should be emphasized that this moderate THD increase is a necessary trade-off to realize effective CMV suppression ($\pm V_{dc}/6$). Effective CMV suppression greatly mitigates bearing currents and electromagnetic interference, bringing promi-

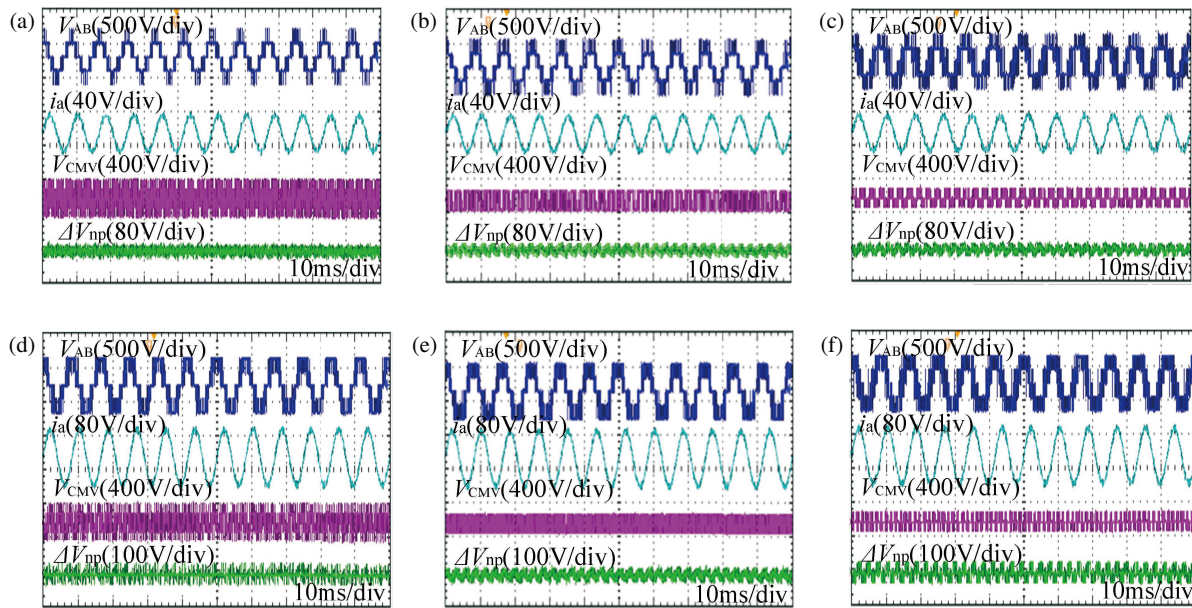


FIGURE 11. Steady-state experimental results of various methods at 1800 r/min with load torques of 30 N·m and 47 N·m, respectively. (a) VSVPWM, $M = 0.65$, (b) IVSVPWM, $M = 0.65$, (c) LVSVPWM, $M = 0.65$, (d) VSVPWM, $M = 0.9$, (e) IVSVPWM, $M = 0.9$, and (f) LVSVPWM, $M = 0.9$.

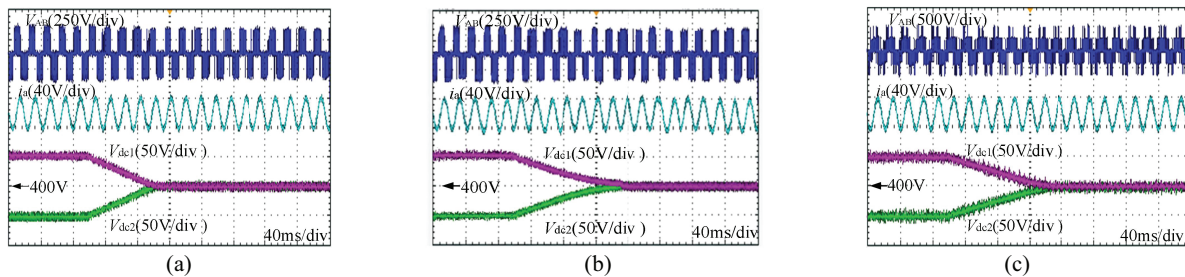


FIGURE 12. Steady-state experimental results of NPV balancing for two methods at $M = 0.3$, 800 r/min, and 30 N·m. (a) VSVPWM, (b) IVSVPWM, and (c) LVSVPWM.

TABLE 4. THD of various methods at different modulation ratios.

M		Method	$THD\ i_a$ (%)	5th (%)	7th (%)	$THDV_{AB}$ (%)
0.3	Fig. 10(a)	VSVPWM	7.21	0.35	0.34	106.85
	Fig. 10(b)	IVSVPWM	7.53	0.46	0.28	126.85
	Fig. 10(c)	LVSVPWM	7.85	0.63	0.08	165.73
0.65	Fig. 11(a)	VSVPWM	4.65	0.26	0.32	58.22
	Fig. 11(b)	IVSVPWM	5.35	0.32	0.34	63.47
	Fig. 11(c)	LVSVPWM	5.19	0.49	0.18	79.78
0.9	Fig. 11(d)	VSVPWM	2.54	0.15	0.11	50.85
	Fig. 11(e)	IVSVPWM	2.86	0.12	0.13	57.34
	Fig. 11(f)	LVSVPWM	2.72	0.06	0.09	62.57

nent long-term reliability advantages for most industrial drive systems.

Table 5 shows the switching count per second for the different methods. One turn-on and one turn-off together count as one switching action. VSVPWM and IVSVPWM both use 9-segment modulation. However, LVSVPWM discards the first or last vector based on current operating conditions; therefore,

its switching count is slightly lower than that of the VSVPWM and IVSVPWM.

Table 6 shows the single-run time consumption of various methods. LVSVPWM exhibits a single-run time of 69.37 μ s, which is 56.9% longer than that of VSVPWM yet 12.4% shorter than that of IVSVPWM, placing it at an intermediate level of computational efficiency.

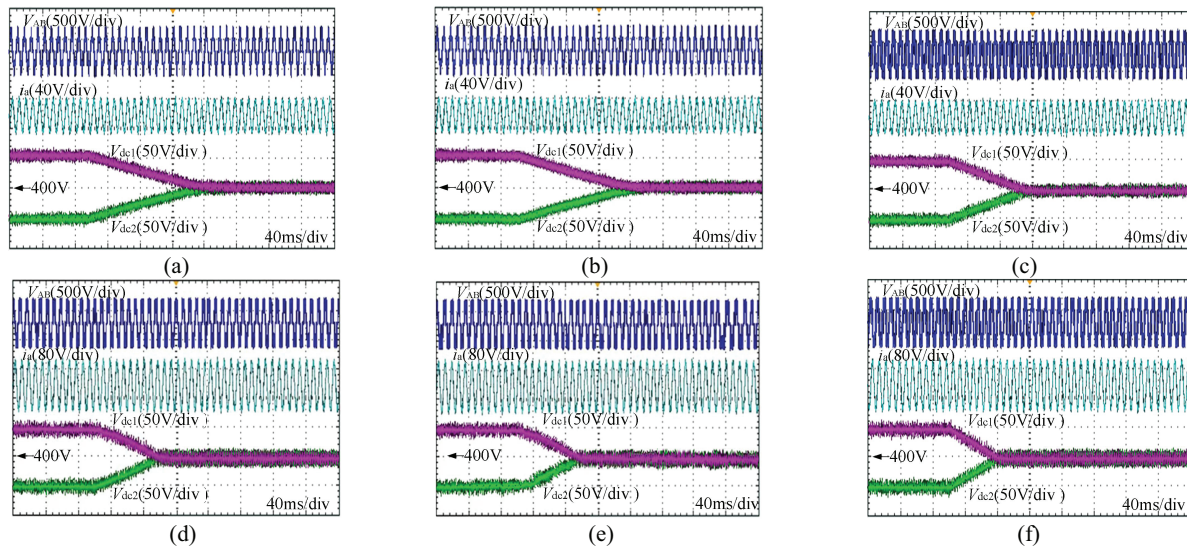


FIGURE 13. Steady-state experimental results of NPV balancing for different methods at 1800 r/min, 30 N·m and 47 N·m. (a) VSVPWM, $M = 0.65$, (b) IVSVPWM, $M = 0.65$, (c) LVSVPWM, $M = 0.65$, (d) VSVPWM, $M = 0.9$, (e) IVSVPWM, $M = 0.9$, and (f) LVSVPWM, $M = 0.9$.

TABLE 5. Switching counts of different methods.

	M	VSVPWM	IVSVPWM	LVSVPWM
Switching count	0.3	80.00K	80.00K	79.08K
	0.65	80.00K	80.00K	78.34K
	0.9	80.00K	80.00K	77.84K

TABLE 6. Single-run time consumption of different methods.

	VSVPWM	IVSVPWM	LVSVPWM
Single-run time consumption	44.20 μ s	74.58 μ s	65.37 μ s

6. CONCLUSION

To address CMV amplification and NPV imbalance in NPC three-level inverters, this study proposes an LVSVPWM method based on VSVPWM for coordinated CMV and NPV suppression. Through experimental analysis under different working conditions, the following conclusions are drawn:

(1) Compared with VSVPWM, the proposed LVSVPWM limits the full-range CMV to $V_{dc}/6$ by removing large CMV vectors. It reduces small sectors via sector reconstruction, cutting sector switching and alleviating side effects including increased harmonics, zero-crossing distortion, and elevated electromagnetic interference.

(2) Compared with VSVPWM and IVSVPWM, the proposed LVSVPWM method breaks the constraint of conventional virtual vector pairs, strengthens the inter-vector correlation, and accelerates the NPV balancing speed. Based on logical judgment, the number of synthesized vectors is reduced, thereby lowering switching commutations and computation time and achieving coordinated control of full-range CMV suppression and NPV balancing.

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