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A Miniaturized High-Efficiency Harmonic-Tuned Class-F Power Oscillator

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ABSTRACT: To address the requirements for compact size and low cost of RF signal sources, a novel design method for high-efficiency Class-F power oscillators is proposed. The key contribution of this method is the integrated design of the harmonic-tuning and impedance-matching networks. An asymmetric π-type harmonic tuning network is proposed to simultaneously realize harmonic termination for high-efficiency Class-F operation and fundamental load impedance matching, thereby significantly reducing circuit footprint. The amplifier's output was coupled to a feedback network via a capacitor and returned to the amplifier through a frequency-selective network, enabling a stable self-excited oscillation. To verify the design, a power oscillator is implemented using a low-cost LDMOS transistor and an FR4 substrate. The experimental results show that the fabricated oscillator operates at 918 MHz with a direct current-to-radio-frequency (DC-RF) efficiency of 68.20% and a maximum output power of 2.90 dBm, robustly validating the effectiveness of this approach.

1. INTRODUCTION

High-efficiency radio-frequency (RF) power generation technology serves as a fundamental cornerstone of modern wireless communication, radar, and microwave energy transmission systems. Among various RF power sources, self-excited oscillators play an indispensable role by converting DC power into stable and high-purity RF microwave signals without requiring external driving sources [1, 2]. Numerous power oscillator designs have been reported in [3–14] and can replace conventional oscillators and driver amplifiers in RF systems, thereby reducing the number of system modules and improving system integration.

With the continuous advancement of wide-bandgap semiconductor technologies and harmonic termination techniques, high-efficiency oscillation can be achieved [15, 16]. Switch-mode power oscillators have been reported in [6–9], where the transistor operates as a Class-E or Class-E/F3 switching device to achieve high efficiency. However, in high-frequency operation, increased switching losses degrade the efficiency of switch-mode power oscillators. In [17–20], Class-F voltage-controlled oscillators (VCOs) were proposed, where the harmonic impedances at the transistor drain terminal are controlled to shape the voltage and current waveforms with reduced overlap, thereby minimizing device power loss and improving efficiency. Nevertheless, the output power of these Class-F VCOs is relatively limited. To achieve medium or higher output power levels, additional power amplifiers are required, which inevitably increase the overall system size and complexity.

On the other hand, harmonic tuning networks are an effective means for power oscillators to achieve high efficiency at elevated operating frequencies. In [11], a harmonic tuning network employing a dual open-circuited stub structure was implemented to shape the current and voltage waveforms into square and half-sinusoidal profiles for the second and third harmonics, respectively, thereby enhancing efficiency. Refs. [12–14] used a $\lambda/4$ short-circuited transmission line at the fundamental frequency (f_o) for second-harmonic control and a $\lambda/12$ open-circuited transmission line at f_o for third-harmonic control to achieve efficiency improvement. Although these recent studies validate the effectiveness of harmonic tuning for efficiency enhancement, they predominantly rely on discrete output matching networks comprising separate harmonic-tuning and fundamental-matching sub-networks. However, such discrete architectures have significant practical limitations: they not only increase structural complexity and footprint — thereby raising fabrication costs — but also introduce undesirable electromagnetic coupling and impedance interactions between harmonic and fundamental paths.

To overcome limitations of conventional harmonic termination networks, including increased circuit complexity and enlarged footprint, this paper presents an integrated harmonic tuning and impedance transformation approach for high-efficiency Class-F power oscillators. The proposed approach is realized by optimizing the conventional harmonic termination network and developing an asymmetric π-type harmonic tuning network. The fundamental distinction from conventional harmonic network topologies is that the proposed network simultaneously provides harmonic termination for Class-F operation and fundamental load impedance transformation, thereby eliminating the requirement for an additional matching network and significantly reducing circuit size. The detailed design procedure of the proposed integrated methodology is presented in the flowchart of Fig. 1. By modifying the topology of the harmonic tuning network, this integrated design methodology can be extended to other classes of harmonic-tuned power oscillators. Under identical transistor, operating frequency, and

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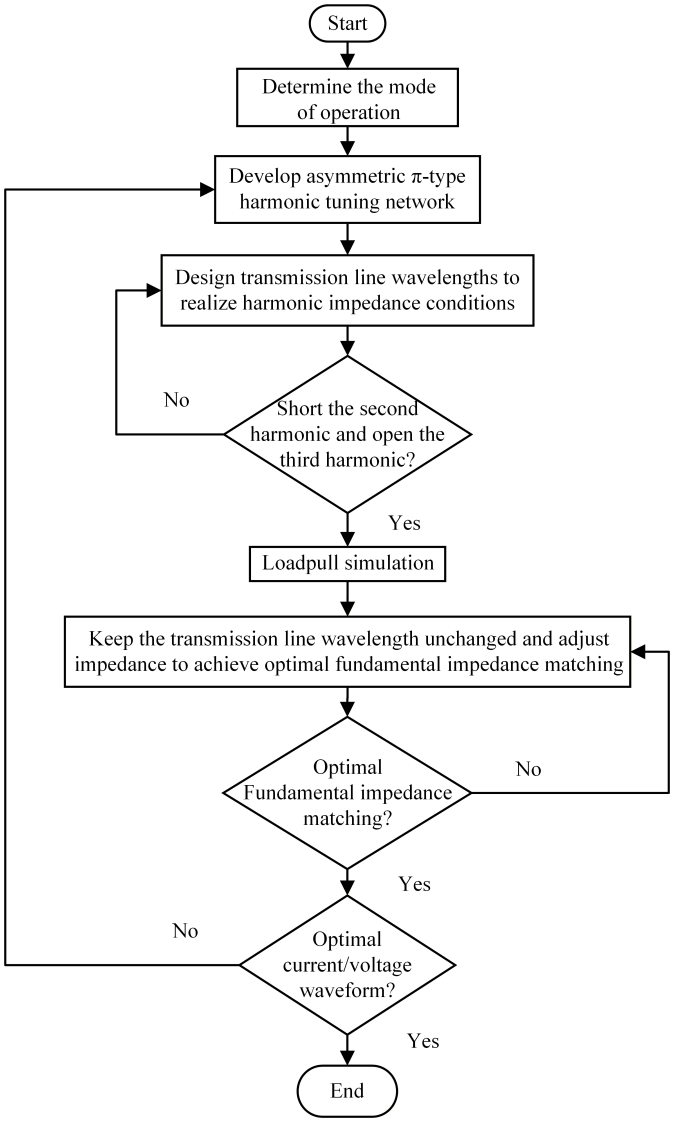

FIGURE 1. The detailed design procedure of the proposed integrated methodology.

bias conditions, the proposed integrated harmonic network can achieve comparable output power and efficiency with the conventional harmonic termination networks. Nevertheless, conventional harmonic termination approaches typically require separate fundamental impedance matching networks, which significantly increase circuit footprint and design complexity. In contrast, the proposed method integrates harmonic termination and fundamental impedance transformation into a single asymmetric π-type network, thereby reducing the overall circuit size while maintaining high-efficiency operation.

2. THEORETICAL ANALYSIS

2.1. Oscillation Conditions of Feedback Oscillators

The power oscillator designed in this study consisted of a power amplifier and feedback network, as shown in Fig. 2. The

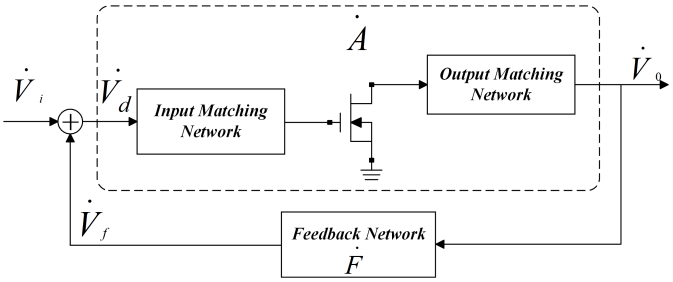

FIGURE 2. Structure of the feedback oscillator.

closed-loop gain of the amplifier is $\dot{A}_f$ expressed as follows:

$$\dot{A}_f \equiv \frac{\dot{V}_o}{\dot{V}_i} \equiv \frac{\dot{V}_o}{\dot{V}_d - \dot{V}_f} \equiv \frac{A}{1 - A\dot{F}} \tag{1}$$

where $\dot{V}_i$ is the applied voltage; $\dot{V}_d$ is the input voltage of the amplifier; $\dot{V}_o$ is the output voltage of the oscillator; $\dot{V}_f$ is the feedback voltage at the output of the feedback network; A is the voltage gain of the open-loop amplifier; and A is the feedback coefficient of the feedback network. According to Barkhausen's criterion, oscillation is established from the inherent thermal noise of the active device. The start-up condition is expressed as

$$|\dot{A}\dot{F}| > 1 \tag{2}$$

The nonlinearity of the active device subsequently limits the oscillation amplitude, driving the system into a steady state. In this regime, the loop must satisfy both the amplitude and phase balance conditions simultaneously, expressed as

$$|\dot{A}\dot{F}| = 1 \tag{3}$$

$$\varphi_A + \varphi_F = 2n\pi \quad (n = 0, 1, 2, \ldots) \tag{4}$$

where φ_A is the phase angle by which $\dot{V}_o$ leads $\dot{V}_d$, and φ_F is the phase angle by which $\dot{V}_f$ leads $\dot{V}_o$.

2.2. Analysis of Class-F Harmonic Tuning Power Oscillators

The operating principle of the proposed Class F power oscillator is based on the harmonic waveform engineering technique employed in conventional Class F power amplifiers. By controlling the harmonic impedances presented to the transistor's drain terminal, the drain voltage and current waveforms can be shaped to minimize their overlap, thereby reducing device power dissipation and improving conversion efficiency. The drain voltage and current waveforms can be expressed by Fourier series as

$$v_{DS}(t) = V_{DC} + \sum_{n=1}^{\infty} V_n \cos(n\omega_0 t + \phi_n) \tag{5}$$

$$i_D(t) = I_{DC} + \sum_{n=1}^{\infty} I_n \cos(n\omega_0 t + \theta_n) \tag{6}$$

where V_n and I_n represent the nth-order harmonic voltage and current components, respectively.

In an ideal Class-F operating mode, the drain voltage waveform approaches a square waveform, while the drain current waveform exhibits a half-sinusoidal shape. Accordingly, the harmonic impedance terminations presented at the transistor drain terminal should satisfy the following conditions to achieve the desired waveform shaping

$$\begin{cases} Z_L(f_0) = R_{\text{opt}} + jX_{\text{opt}}, \\ Z_L(2nf_0) = 0, \quad n = 1, 2, 3 \ldots, \\ Z_L\left((2n+1)f_0\right) = \infty, \quad n = 1, 2, 3 \ldots. \end{cases} \tag{7}$$

In practical designs, the ideal Class-F operation can be approximately achieved by controlling only second-harmonic short-circuit and third-harmonic open-circuit conditions. Therefore, the drain voltage waveform consists of the DC component, the fundamental component, and the third-harmonic component, while the drain current waveform is composed of the DC component and the second-harmonic component, which can be expressed as

$$v_{\text{ds}}(t) = V_{\text{dc}} + V_1 \cos \omega_0 t + V_3 \cos 3\omega_0 t \tag{8}$$

$$i_{\text{d}}(t) = I_{\text{dc}} - I_2 \cos 2\omega_0 t \tag{9}$$

In practical circuits, ideal harmonic termination conditions cannot be perfectly achieved due to transistor parasitic effects, transmission-line losses, and other nonidealities. Therefore, the harmonic impedances can only approximate the ideal short-circuit and open-circuit conditions, resulting in an actual efficiency lower than the theoretical limit.

2.3. The Asymmetric π-Type Harmonic Tuning Network Structure

In conventional Class-F designs, the harmonic tuning network and fundamental impedance-matching network are independently developed, resulting in unwanted impedance interaction and electromagnetic coupling between the two networks, as well as an increased circuit footprint. To overcome these limitations, this work proposes a dual-parameter decoupling methodology based on independently manipulating electrical length and characteristic impedance, enabling the integration of harmonic termination and fundamental impedance transformation within a single asymmetric π-type topology.

Figure 3 illustrates the proposed asymmetric π-type harmonic-tuning network. Among them, a $\lambda/4$ short-circuited microstrip line at f_o, TL_1, presents a short-circuit impedance at the second harmonic ($2f_o$) at node A, while simultaneously serving as the drain-bias feed. A $\lambda/12$ open-circuited microstrip line at f_o, TL_3, presents a short-circuit impedance at the third harmonic ($3f_o$) at node B. Finally, a $\lambda/4$ microstrip line at f_o, TL_2, transforms the short-circuit impedance at node B into open-circuit at node A for $3f_o$, thereby realizing ideal Class-F harmonic terminations.

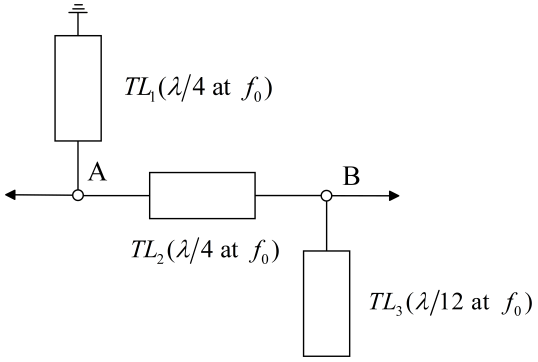

FIGURE 3. The asymmetric π-type harmonic tuning network structure.

Through iterative optimization based on load-pull and source-pull simulations in Keysight Advanced Design System (ADS), the transistor's optimal fundamental load impedance, $Z_{L\text{opt}}$, was determined to be 5.4+j7.36 by selecting the peak-efficiency point from load-pull simulation results plotted in Fig. 4. Fig. 5 illustrates the fundamental load-impedance transformation schematic of the asymmetric π-type harmonic-tuning network. Among them, TL_3 is a shunt open-circuited microstrip line. The input impedance Z_{in3} looking into TL_3 from node B is formulated as

$$Z_{in3} = -jZ_3 \cot(\theta_3) \tag{10}$$

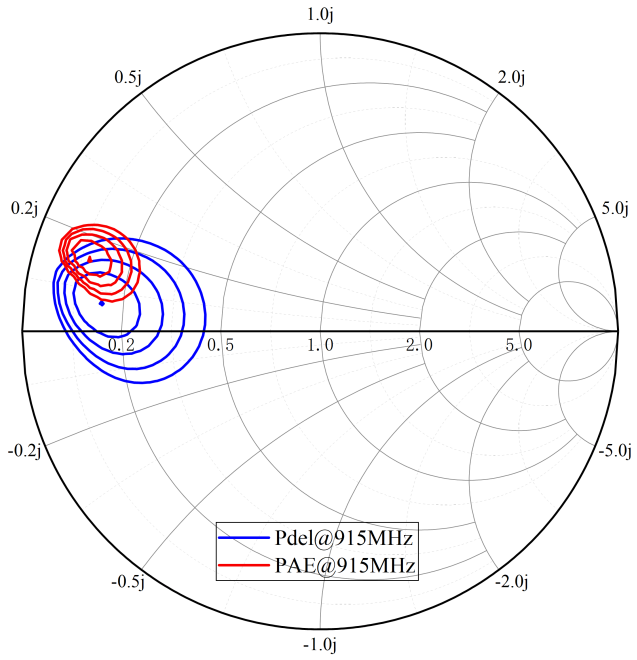

FIGURE 4. Simulated Smith chart trajectory of the fundamental load impedance.

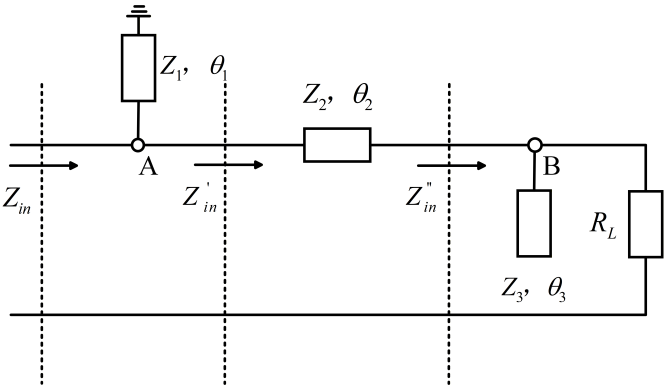

FIGURE 5. The fundamental load impedance transformation schematic of the asymmetric π-type harmonic tuning network.

The load impedance Z''_{in} of TL_2 is the parallel combination of the input impedance Z_{in3} of TL_3 and the impedance of R_L

$$Z''_{in} = \frac{1}{Z_{in3}} + \frac{1}{R_L} \tag{11}$$

The input impedance Z'_{in} looking into the left side of TL_2 is given by

$$Z'_{in} = Z_2 \frac{Z''_{in} + jZ_2 \tan(\theta_2)}{Z_2 + jZ''_{in} \tan(\theta_2)} \tag{12}$$

TL_1 acts as a shunt short-circuited microstrip line. The input impedance Z_{in1} looking into TL_1 from node A is given by

$$Z_{in1} = jZ_1 \tan(\theta_1) \tag{13}$$

Node A is the junction where TL_1 and TL_2 are connected in parallel, and its input impedance Z_{in} is given by

$$Z_{in} = \frac{Z_{in1} \cdot Z'_{in}}{Z_{in1} + Z'_{in}} \tag{14}$$

To satisfy the harmonic tuning conditions of Class-F power oscillators, electrical lengths θ_1, θ_2, and θ_3 of microstrip lines TL_1, TL_2, and TL_3 were fixed at 90°, 90°, and 30° at f_o, respectively. By substituting $Z_{in} = Z_{Lopt}$ into Equation (14), the unique characteristic impedances Z_2, and Z_3 for TL_2, and TL_3 were calculated to be $16.4\,Omega$ and $21.2\,Omega$, respectively. TL_1 functions as the $\lambda/4$ short-circuited microstrip line at f_o. It does not participate in fundamental load-impedance matching; instead, it serves as the drain-bias feed line, and its characteristic impedance Z_1 was set to $50\,Omega$. Ultimately, three key conditions of the asymmetric π-type harmonic tuning network illustrated in Fig. 6 are simultaneously satisfied at node A: (1) fundamental frequency matching, (2) second-harmonic approximate short circuit, and (3) third-harmonic approximate open circuit.

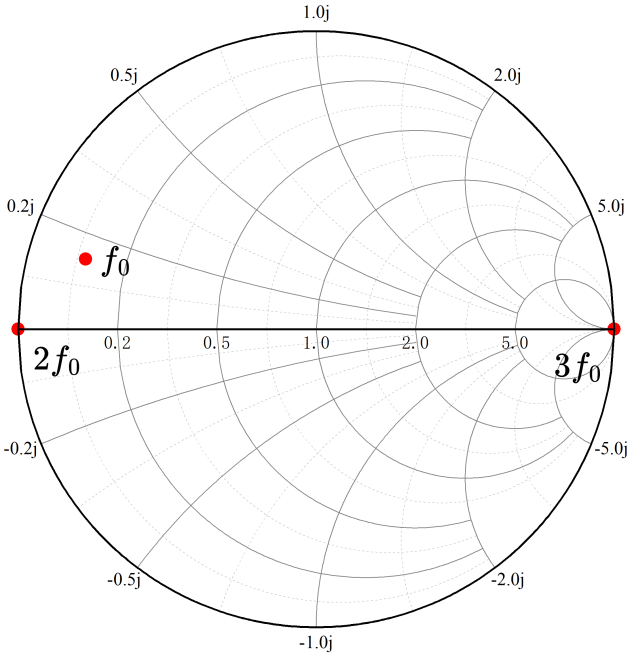

FIGURE 6. Smith chart representation of the fundamental and harmonic impedance distribution for the asymmetric π-type harmonic tuning network.

The electrical lengths and characteristic impedances of TL_1, TL_2, and TL_3 are determined by their physical lengths and widths, respectively. Dimensional variations of these transmission lines directly affect the harmonic impedance terminations and fundamental impedance transformation characteristics. Specifically, deviations in line length result in phase errors of the harmonic terminations, causing second- and third-harmonic impedances to deviate from ideal Class-F conditions. Consequently, the drain voltage and current waveforms are distorted, leading to degraded output power and efficiency. In contrast, variations in line width primarily alter the characteristic impedance, which affects fundamental impedance matching and oscillation frequency. Severe dimensional deviations may further disturb the Barkhausen oscillation condition and prevent stable startup. Therefore, the accurate control of microstrip dimensions is essential for fabrication tolerance and robustness of the proposed asymmetric π-type harmonic tuning network.

3. DESIGN OF HIGH EFFICIENCY POWER OSCILLATORS

3.1. Simulation of the High-Efficiency Class-F Power Amplifier

A 915 MHz ISM band was selected due to its reduced free-space path loss and enhanced penetration capability compared to the 2.45 GHz band. This frequency enables lower atmospheric attenuation and superior RF-to-DC conversion efficiency, thereby facilitating long-range RF energy harvesting for devices.

To achieve a high conversion efficiency in the power oscillator at the target frequency, the design of the high-efficiency Class-F power amplifier shown in Fig. 7 is a critical preliminary step. On the output side, TL_1, TL_2 and TL_3 constitute the asymmetric π-type harmonic-tuning network, where TL_4 serves as the tuning line and C_2 is the DC-blocking capacitor. The circuit on the left side of the LDMOS transistor functions as an input-matching network, with an additional DC-blocking capacitor C_1 incorporated to prevent DC leakage.

The overall matching performance of the complete amplifier (PA) circuit is characterized by the curve shown in Fig. 8(a). The simulated input return loss at 915 MHz was below -20 dB, indicating good impedance matching. Fig. 8(b) shows the simulated output power, gain, and power-added efficiency (PAE) as functions of input power, under a gate voltage of 2.0 V, a drain voltage of 28 V, and an input power of 27 dBm. At 915 MHz, the simulated PAE reached a peak value of 75.67%, with a corresponding output power of 43.08 dBm.

3.2. Implementation of the Feedback Network

To improve the oscillator's phase noise performance and frequency selectivity, while considering its narrow operating bandwidth and minimizing the influence of the feedback network on the harmonic-tuning network, a stepped-impedance bandpass filter was used in this work, as shown in Fig. 9(a).

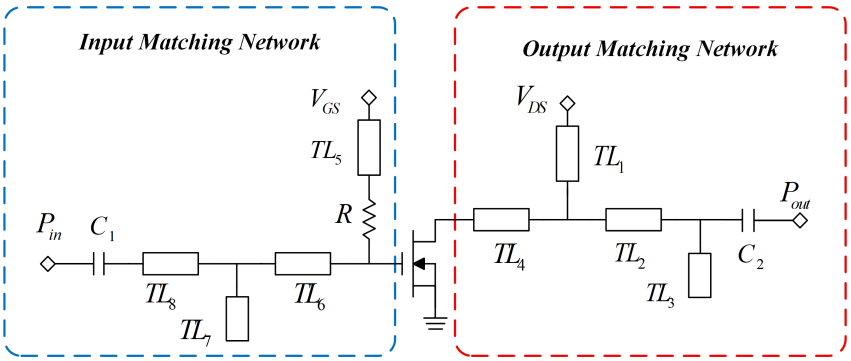

FIGURE 7. Circuit schematic of the high-efficiency Class-F power amplifier.

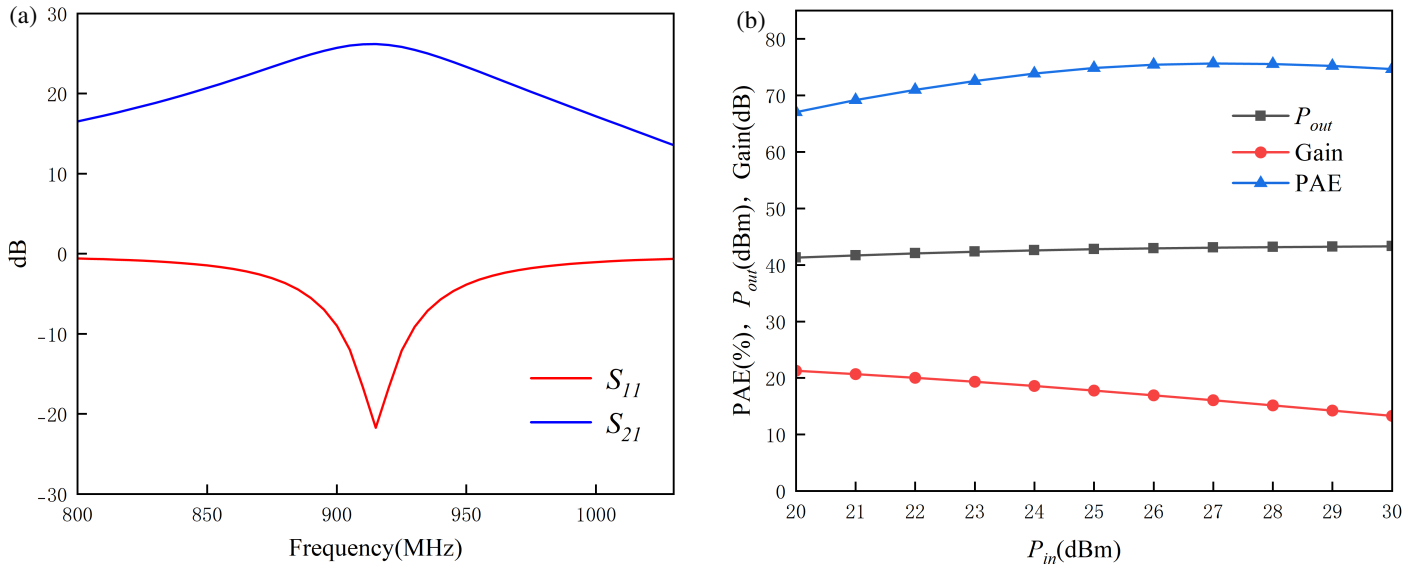

FIGURE 8. (a) Simulated results demonstrating the matching performance and (b) simulated output power, gain, and PAE versus input power.

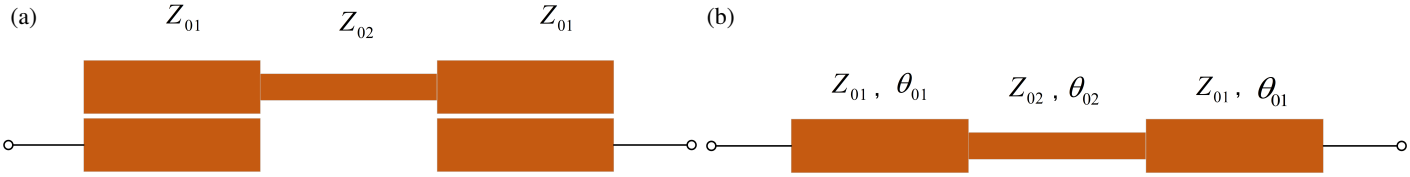

FIGURE 9. (a) Schematic of the stepped-impedance bandpass filter and (b) structure of the stepped-impedance resonator.

This bandpass filter consists of a stepped-impedance resonator (SIR) and parallel-coupled lines,and the parallel-coupled lines are located at both ends of the SIR. The resonator structure is illustrated in Fig. 9(b).

In accordance with the topology of the stepped-impedance bandpass filter, this filter was designed using microstrip lines in Advanced Design System (ADS). To minimize the SIR size and enhance harmonic suppression, the characteristic impedances Z_{01} and Z_{02} were increased, while the impedance ratio $K = \frac{Z_{01}}{Z_{02}}$ was reduced. The coupling strength between SIR and parallel-coupled lines can be improved by reducing the intermediate coupling gap. The characteristic impedances Z_{01} and Z_{02} were set to 50 Ω and 75 Ω, respectively, and the coupling gap was fixed at 0.1 mm. Finally, to ensure fundamental frequency transmission while suppressing harmonic components, electrical lengths θ_{01} and θ_{02} of the two microstrip lines were determined to be 50° and 48°, respectively, via ADS simulation and parametric optimization.

Figure 10 depicts simulated S_{11} and S_{21} of the designed stepped-impedance bandpass filter at the fundamental, second-harmonic, and third-harmonic frequencies, with magnitudes expressed in dB. The simulation results indicate that the filter allows the fundamental frequency to pass through while effectively suppressing the second and third harmonics. To compen-

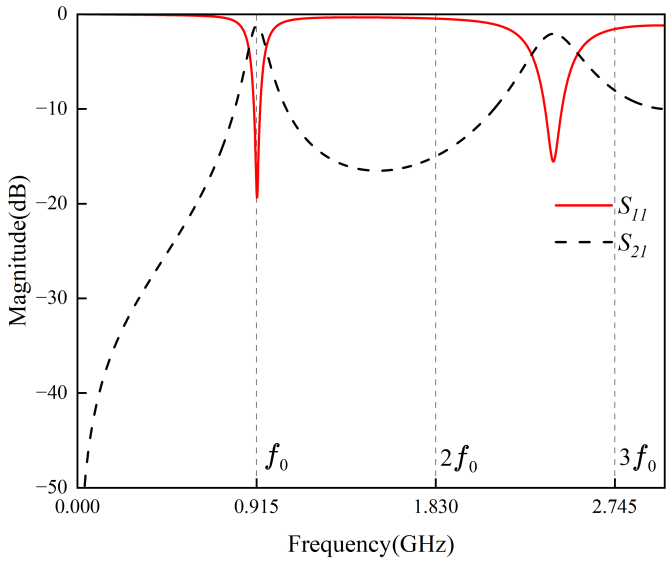

FIGURE 10. Simulated results of the stepped-impedance bandpass filter at the fundamental, second-harmonic, and third-harmonic frequencies.

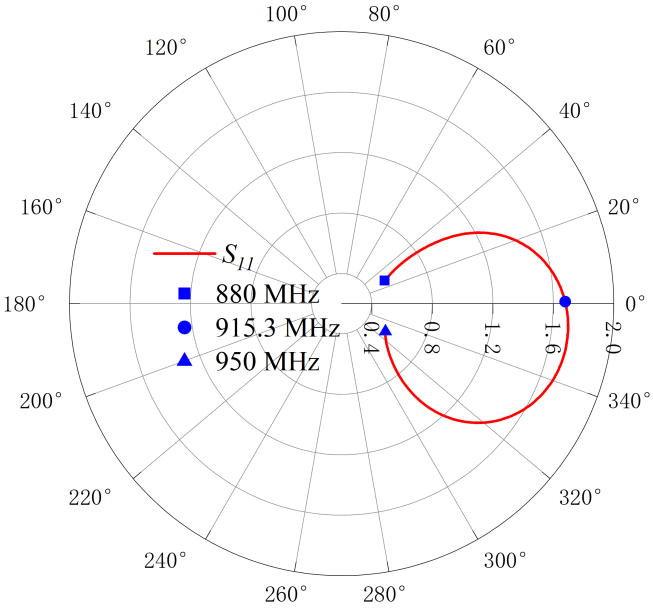

FIGURE 11. Simulation result of the closed-loop circuit S_{11}.

sate for the phase delay between amplification and feedback circuits, two 50 Ω phase-delay lines were added on both sides of the stepped-impedance bandpass filter. To facilitate robust self-oscillation, a coupling capacitor injects the PA output signal into the feedback path, which is routed through the stepped-impedance bandpass filter and the phase-delay lines before being delivered to the PA input, thereby establishing the closed-loop circuit.

As illustrated by the simulated S_{21} response in Fig. 10, the bandpass filter achieves an insertion loss below 1.2 dB within the operating frequency range of 910–920 MHz, with a minimum loss of 1.1 dB at the center frequency of 915 MHz. The in-band loss introduced by the bandpass filter in the feedback loop inevitably dissipates a portion of the RF energy, thereby reducing the available output power and degrading the overall DC-to-RF efficiency of the proposed oscillator.

For stability analysis of the feedback oscillator, an OscTest control was incorporated into the closed-loop circuit. The OscTest control integrates the loop gain into a single S-parameter; in this study, S_{11} was selected for simulation, with the results illustrated in Fig. 11. As observed from the polar plot, the S_{11} curve of the closed-loop circuit encircles the point $1+j0$. Moreover, near the frequency of 915.3 MHz, the magnitude of S_{11} exceeds 1, and the corresponding phase is approximately 0° (i.e., $2n\pi$, where $n = 0$), satisfying the Barkhausen oscillation criterion. Therefore, the closed-loop circuit was verified to be self-oscillating.

3.3. Complete Design of the Power Oscillator

A complete schematic of the proposed power oscillator is shown in Fig. 12. The harmonic tuning network ensures short-circuit termination at f_2, open-circuit termination at f_3, and proper fundamental load impedance matching. A series resistor was included in the gate bias network to stabilize the transistor's quiescent operating point. To suppress low-frequency parasitic oscillations and achieve power supply decoupling, bypass capacitors ranging from picofarads to microfarads were integrated into both the gate and drain bias networks. Specifically, picofarad-range capacitors were positioned adjacent to the transistor footprint to provide a low-impedance path for high-frequency RF currents. This configuration effectively shunts RF energy to ground, thereby preventing bias-line contamination and mitigating parasitic resonances within the bias network. In contrast, microfarad-range capacitors were implemented to suppress low-frequency power-supply ripples and ensure DC bias stability by maintaining a constant voltage potential at the bias port. Additionally, one capacitor was placed on each side of the stepped-impedance bandpass filter; adjusting the capacitance values introduces phase variations in the feedback loop, thereby enabling fine-tuning of the oscillation frequency.

Oscillator's simulated drain voltage and current waveforms at an operating frequency of 915 MHz are shown in Fig. 13. Compared with the ideal Class-F waveform, certain distortions were observed. These deviations were primarily attributed to inaccuracies in the nonlinear transistor model provided by the manufacturer.

Simulated phase noise characteristics of the proposed oscillator are presented in Fig. 14. At frequency offsets of 10 kHz, 100 kHz, and 1 MHz from the oscillation frequency, the simulated phase noise values are −102.90 dBc/Hz, −122.90 dBc/Hz, and −140.91 dBc/Hz, respectively. The excellent phase-noise performance verifies the effectiveness of the proposed stepped-impedance bandpass filter in suppressing phase fluctuations and improving the spectral purity of the self-excited oscillator.

The oscillator can be custom-tailored for a specific target frequency by optimizing fundamental load impedance, tuning the microstrip line operating frequency within the asymmetric π-type harmonic-tuning network, and adjusting the feedback loop to satisfy Barkhausen oscillation criterion.

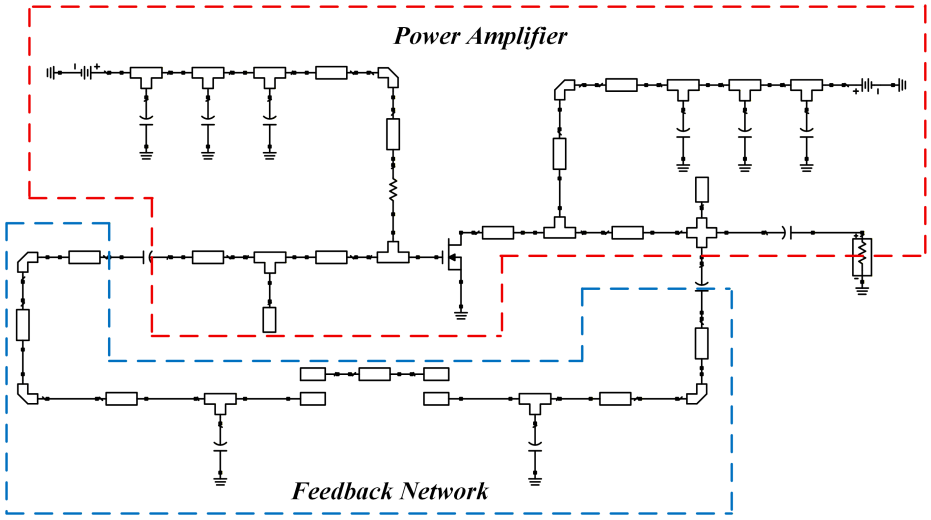

FIGURE 12. Complete schematic of the proposed high-efficiency power oscillator.

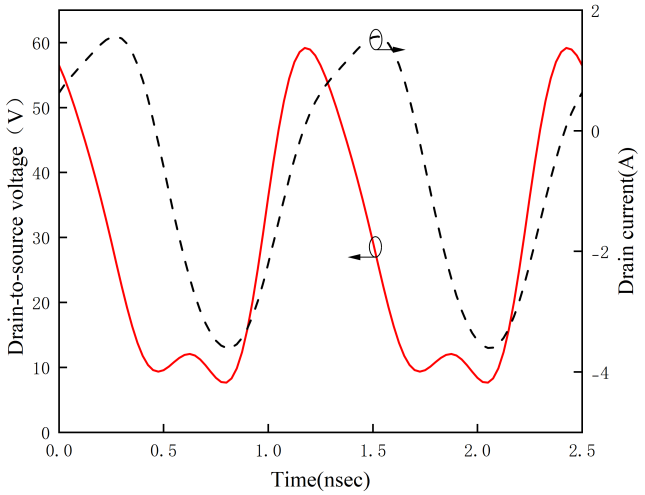

FIGURE 13. Simulated drain voltage (V) and current (A) waveforms of the power oscillator at 915 MHz.

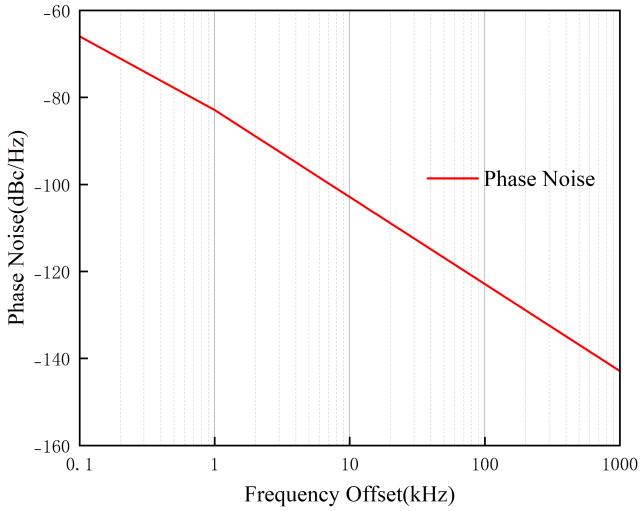

FIGURE 14. Simulated phase noise of the power oscillator.

4. EXPERIMENTAL VERIFICATION AND ANALYSIS

To verify the effectiveness of the proposed design approach, a 915 MHz power oscillator was implemented on a 1-mm-thick FR4 substrate with a dielectric constant of 4.4. The fabricated prototype is shown in Fig. 15. The circuit occupies an area of 100 mm $\times$ 70 mm, and an aluminum backplate is attached to the bottom of the substrate for thermal management.

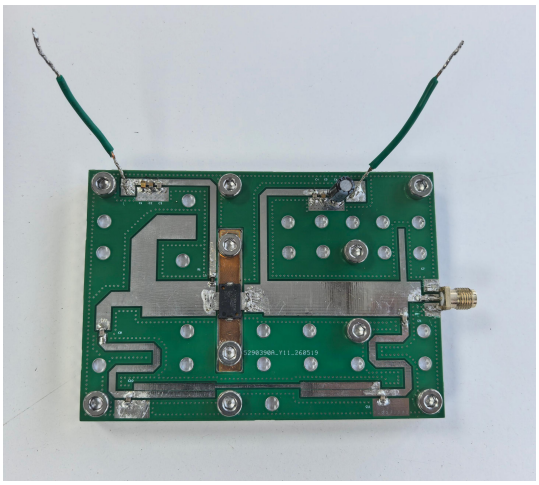

FIGURE 15. Photograph of the fabricated power oscillator.

The experimental characterization was carried out using a DC power supply, attenuators, RF isolators, and a spectrum analyzer. Before measurement, the attenuators and spectrum analyzer were calibrated to eliminate systematic errors. The fabricated power oscillator was then connected to the test setup. Biasing was applied sequentially: the gate bias was first supplied to the LDMOS transistor, followed by the drain bias. Upon successful turn-on, the oscillator entered steady-state oscillation. Once the spectral response on the spectrum analyzer stabilized, the DC power consumption, oscillation frequency, and output power were recorded. The output power P_{out} was calculated by summing the power reading from the spectrum analyzer and

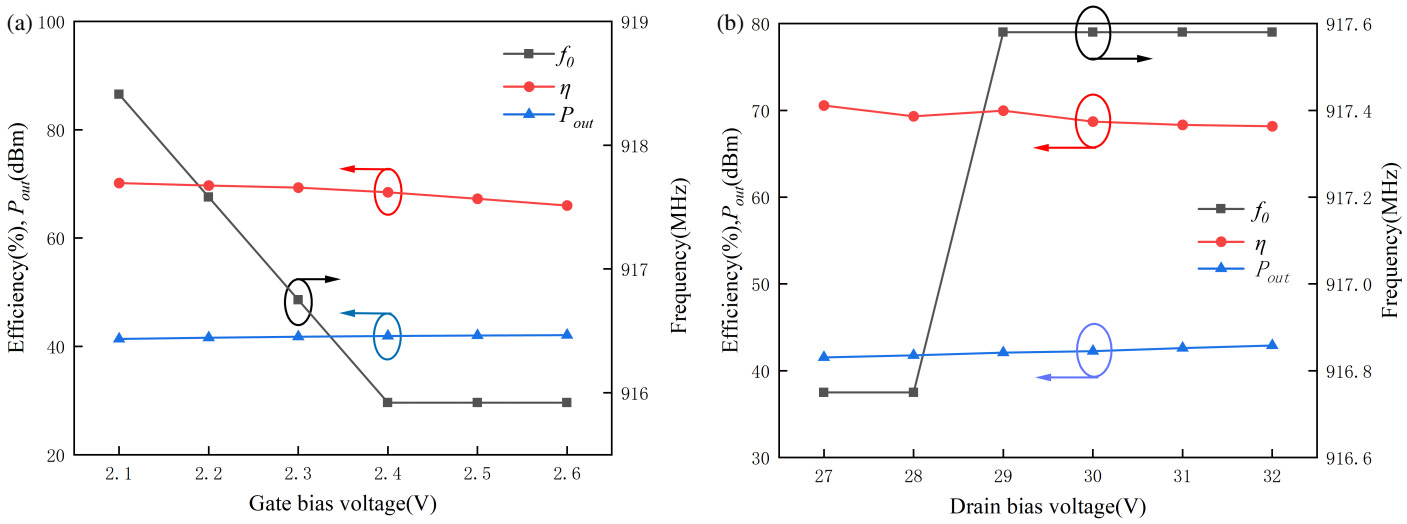

FIGURE 16. Measured DC-to-RF conversion efficiency (η), output power (P_{out}), and oscillation frequency (f_0) as a function of (a) gate bias voltage at a drain bias voltage of 28 V and (b) drain bias voltage at a gate bias voltage of 2.3 V.

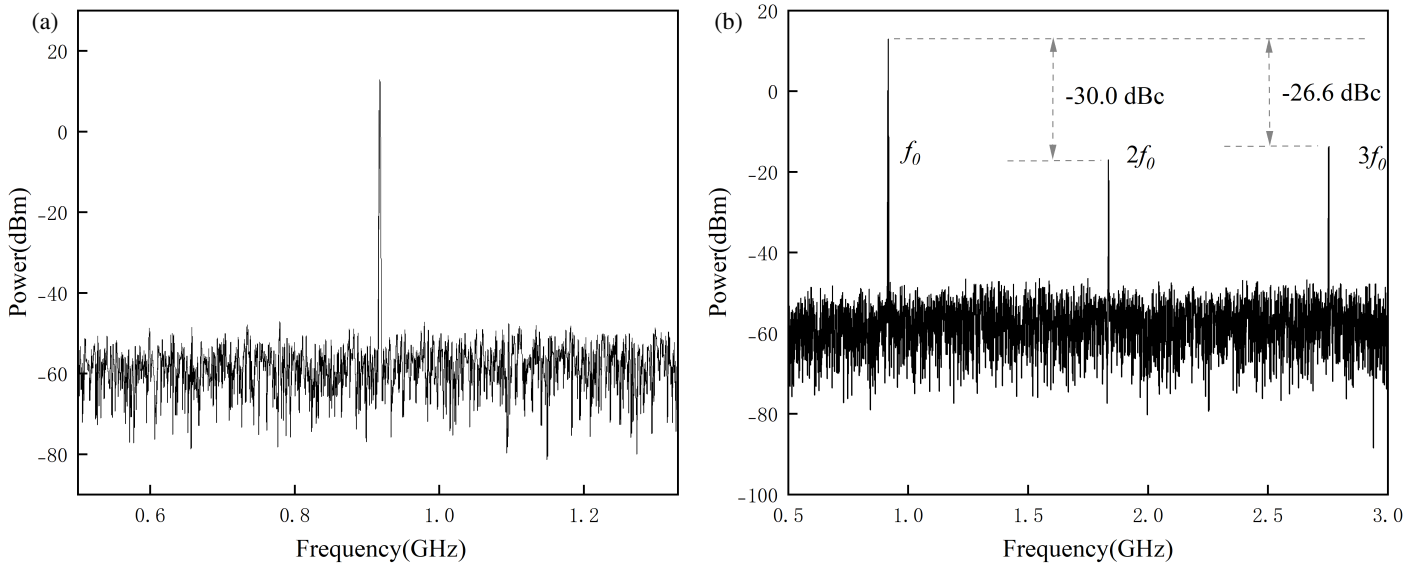

FIGURE 17. Measured output spectra of the proposed oscillator under the maximum output power bias condition (V_{GS} = 2.3 V and V_{DS} = 32 V) with a 30-dB external attenuator: (a) fundamental output spectrum and (b) second- and third-harmonic output spectra.

the attenuator's insertion loss. The DC-to-RF conversion efficiency η was then evaluated as

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}} \times 100\%, \tag{15}$$

where P_{DC} denotes the DC power consumption measured at the supply terminals. During measurement, phenomena such as failure to oscillate or frequency deviation from the designed value were also observed and documented for further analysis.

In this work, the output power and oscillation frequency of the proposed oscillator were experimentally characterized using a Ceyear 4082F signal and spectrum analyzer. Fig. 16 illustrates the variations in P_{out}, η, and oscillation frequency f_0 with respect to gate voltage V_{GS} and drain voltage V_{DS}. In Fig. 16(a), when V_{DS} is 28 V, V_{GS} varies from 2.1 to 2.6 V, resulting in only a few MHz changes in the oscillation frequency, indicating good frequency stability. The output power variation was only a few dB because the transistor operates primarily in the saturated power region. As shown in Fig. 16(b), the output power was relatively sensitive to changes in V_{DS}, which is consistent with the characteristics of a PA.

Figure 17(a) shows the measured output spectrum of the proposed oscillator under maximum output power bias condition (V_{GS} = 2.3 V and V_{DS} = 32 V), where a 30-dB external attenuator was used to protect the measurement instrument. Fig. 17(b) shows the measured output power spectra of the second- and third-order harmonics under the same operating condition. At the oscillation frequency of 918 MHz, the proposed oscillator delivers a maximum output power of

TABLE 1. Performance comparison table for power oscillators.

Ref.	Year	Technology /supply(V)	Substrate	f_0 (GHz)	η	P_{out} (W)	Class	Size ($L \times W$ mm)	Circuit complexity
[8]	2022	GaN/25	-	0.433	67%	64	Class-E	-	High
[9]	2024	MOS/4.5	-	0.0008	93.5%	1.02	Class-E/F_3	-	Medium
[12]	2012	GaN/22	TLX-7	2.42	80.2%	3.2	Harmonic-tuned	50×100	Medium
[13]	2015	GaN/30	TLX-7	2.45	83%	6.1	Harmonic-tuned	60×110	Medium
[14]	2022	GaN/28	FR-4	2.45	72%	5.88	Harmonic-tuned	27×49	Low
[21]	2026	GaN/28	Rogers	2.46	81.6%	10.1	Harmonic-tuned	61×53.5	Medium
This work	2026	LDMOS/32	FR-4	0.918	68.2%	19.5	Class-F	100×70	Low

42.9 dBm with a corresponding DC-to-RF conversion efficiency of 68.2%. Due to the relatively high dielectric loss of the adopted FR-4 substrate, harmonic suppression performance is degraded. In practical engineering applications, a bandpass isolator (or circulator) can be mounted at the output port of power amplifiers and oscillators. This component not only protects the transistor from reflected power but also enhances oscillation frequency stability against load variations; furthermore, it provides additional attenuation of harmonic components.

The stability performance of the proposed Class-F power oscillator was further evaluated via experimental measurements, including startup behavior and long-term operational stability. During the startup test, the drain supply voltage was applied before the gate bias voltage, and the gate voltage was slowly increased. The oscillator achieved instantaneous startup when V_{DS} exceeded 2.0 V, indicating sufficient loop gain and proper phase conditions of the feedback network. Under steady-state operating conditions with fixed bias voltages, the oscillation frequency and output power remained highly stable with only minor variations. Due to the high output power, the temperature of the heat sink and external attenuator increased after several hours of continuous operation. Nevertheless, the oscillation frequency fluctuated within a few kHz and the output power decreased by only several tenths of dBm. These experimental results verify excellent frequency stability, thermal robustness, and long-term reliability of the proposed Class-F power oscillator.

Table 1 summarizes the key performance metrics of harmonic-tuned power oscillators reported in recent literature. The comparative analysis reveals that the proposed power oscillator delivers high efficiency within the 915 MHz operating band. By adopting an FR-4 substrate and an LDMOS transistor, the proposed design achieves the lowest fabrication cost among the referenced designs, thereby well satisfying the requirement for low-cost signal sources in systems. It delivers an output power of 19.5 W, offering sufficient power to satisfy the demands of high-power wireless energy transmission applications. A DC-to-RF conversion efficiency of 68.2% is achieved, minimizing power dissipation and enhancing the overall system efficiency. Furthermore, the proposed oscillator exhibits a distinct compact-size advantage, facilitating its integration into systems.

5. CONCLUSION

This paper presents the design and implementation of a high-efficiency Class-F power oscillator for RF power source applications. First, an asymmetric π-type harmonic-tuning network was developed. This network not only shapes the voltage and current waveforms to achieve Class-F operation for high efficiency but also performs fundamental impedance matching while significantly reducing circuit size. Based on this, a high-efficiency power amplifier was designed and fabricated using an LDMOS device, as the oscillator's sustaining stage. The standalone amplifier achieved an output power of 43.08 dBm and power-added efficiency (PAE) of 75.67% at 915 MHz. Subsequently, leveraging the above amplifier, a high-efficiency power oscillator was realized. The feedback network is constructed using a coupling capacitor, phase delay line, and stepped bandpass filter to satisfy the Barkhausen criterion. Measurement results show that under a gate bias of 2.3 V and a drain bias of 32 V, the proposed oscillator at 918 MHz delivers an output power of 42.90 dBm with a DC-RF efficiency of 68.20%. The final physical dimensions of the proposed oscillator are 100 mm $\times$ 70 mm.

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